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Proposal of a Planar $8F^2$ 1T2C-Type Ferroelectric Memory Cell

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1. Introduction

FeRAM (ferroelectric random access memory) is one of the most promising memories used in portable electronic devices. So far, two types of FeRAM cells have been proposed; one is a capacitor-type or 1T1C-type cell which is composed of an FET and a ferroelectric capacitor, and the other is an FET-type or 1T-type cell which is composed of a single ferroelectric-gate FET. The latter cell has an advantage that stored data can be read out non-destructively. However, there is a significant problem in the 1T-type cell that the data retention time is short. In order to solve this problem, a 1T2C-type cell has been proposed, in which two ferroelectric capacitors with the same area are connected to the gate electrode of a MOSFET [1], and the basic operation of the cell has been demonstrated [2]. In this paper, a novel method to write a datum in a selected cell in the 1T2C array is discussed and then we propose a novel cell structure which is suitable for high density integration.

2. Basic operation of 1T2C-type ferroelectric memory

The cell structure and the polarization directions of the ferroelectric capacitors are shown in Fig.1. In order to write a datum in this cell, a positive or negative pulse is applied between the terminal A and B, so that the two ferroelectric films are polarized oppositely with respect to the gate electrode of MOSFET. In this case, the electric charges induced to the electrodes of both capacitors are canceled each other and no charge is induced to the gate electrode of FET, which means that no depolarization field is generated in the ferroelectric film, and the retention time as long as that of the usual 1T1C-type memory can be expected.

For the "readout" operation, positive voltage pulses are applied to the terminal B, keeping the terminal A open. In this operation, when the stored datum is "0", no polarization reversal occurs in the ferroelectric film and a little drain current flows through the MOSFET, assuming an enhancement type n-channel FET. To the contrary, when the stored datum is "1", the polarization of C_{FB} is reversed and a large drain current flows.

3. Memory cell structure with parallel electrodes

In order to integrate these cells, an array structure shown in Fig. 2 is proposed [1]. In the data writing method, the MOS gate capacitance C_{OX} of 1T2C cell is assumed to be negligibly small and a voltage pulse is applied between the first and second metal electrodes. However, in the actual structure, the gate capacitance is not very small. Under such a condition, the appropriate voltages are not applied to the both capacitors. In the worst case, the polarization of the ferroelectric capacitor is reversed undesirably.

Thus, we proposed an alternative data writing method and array structure shown in Fig. 3 [4], which is applicable to the case where the MOS gate capacitance is not negligible. In this structure, C_{FA} and C_{FB} are formed between the two metal electrodes and the floating gate. In order to write a datum "1" in a selected cell in the array, a positive voltage pulse is applied to the selected metal electrode forming C_{FA}, keeping the selected Si stripe grounded, and in the next timing, a negative pulse is applied to the selected metal electrode forming C_{FB}, keeping the same Si stripe grounded. At the same time, voltage pulses satisfying the V/3 rule are applied to other metal electrodes and Si stripes, in order to minimize the "data disturb" effect. This data writing method is summarized in Fig. 4, in which the above mentioned method has been realized using only positive voltage pulses. As can be seen from the figure, the compensation effect giving bipolar pulses with the same amplitude is automatically realized in almost all non-selected cells, except for non-selected cells located along the selected metal electrodes.

4. $8F^2$ cell configuretion

In Fig. 3, the minimum cell area is $16F^2$ (F : minimum feature size), because both the transistor length and the floating gate width including the spacing of each cell are longer than 4F. In this paper, we propose a novel cell structure in which depletion type p-channel FETs are connected in series along a Si stripe on an insulating substrate, as shown in Fig. 5. In this structure, the gate length which is covered with a floating gate electrode is 3F and the gate width is F. Thus, the minimum cell area is $8F^2$, as shown in Fig.5 (b). The structure on the floating gate is the same as that in Fig. 3. In order to write data in these cells, positive or negative voltages are applied between the selected Si stripe and the selected metal electrode in the same manner as Fig. 4. The "readout" operation is also similar to the previous cases. In this case, however, the source-drain resistance becomes high due to polarization reversal of a ferroelectric film, which is essential in series connection of FETs. The structure can be fabricated using self-aligned technique.

Figure 6 shows a SPICE simulation result of a 1×3 array of $8F^2$ cell. The circuit configuration is depicted in Fig. 7. A 0.07μm-gate length technology was assumed for simulating the operation of FETs. Gate-length L and gate-width W were assumed to be 0.21μm and 0.07μm, respectively. In calculation of ferroelectric components, the simulation model developed by T. Tamura *et al.* was used [5]. Remnant polarization Pr of $10\mu C/cm^2$, coercive voltage Vc of 1.1V, and area of $0.0049\mu m^2$ were assumed as simulation parameters of ferroelectric capacitors. In this simulation a "readout" pulse voltage as low as V/2 was assumed. The actual V value was 3V and the drain voltage of -0.1V was assumed during the "readout" operation.

At first, "1", "0" and "1" are written in the cell 1, 2 and 3, respectively. Next, 5 reading pulses are applied to the terminal B of each cell sequentially, keeping terminal A open. When the "write" operation is completed, polarization charges $Q_{ferro}(\mu C/cm^2)$ of ferroelectric capacitors A and B have almost the same absolute values, which are sufficiently large to memorize the information "0" or "1" safely, and the polarized directions are opposite each other. Consequently, the floating gate voltage V_{fg} (V) becomes almost zero and no

depolarization field is expected to generate in the ferroelectric capacitor. Concerning the "readout" operation, the figure shows that non-destructive readout can be carried out. Furthermore, as we can see the readout current ratio I_{ds}(datum"1")/I_{ds}(datum"0") over 3 orders of magnitude is successfully obtained, as indicated in the figure.

5. Conclusions

We proposed and simulated a planar $8F^2$ 1T2C-type FeRAM cell. It was shown from the simulation results that the ferroelectric films were well polarized in this method, even if the gate capacitance was relatively large. It was also shown that the written data could be readout non-destructively with the current on/off ratio over 3 orders of magnitude.

References

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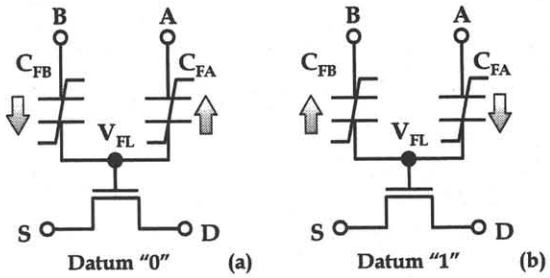

Fig. 1. 1T2C-type ferroelectric memory cell.

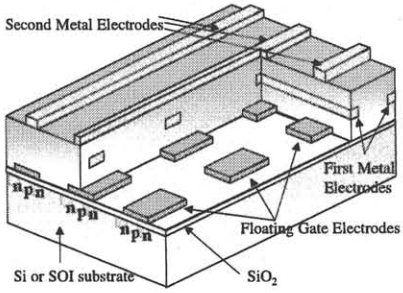

Fig. 2. A 1T2C-type ferroelectric memory array.

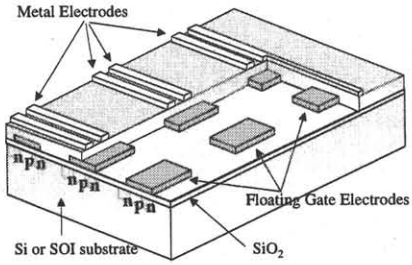

Fig. 3. A novel 1T2C-type ferroelectric memory array.

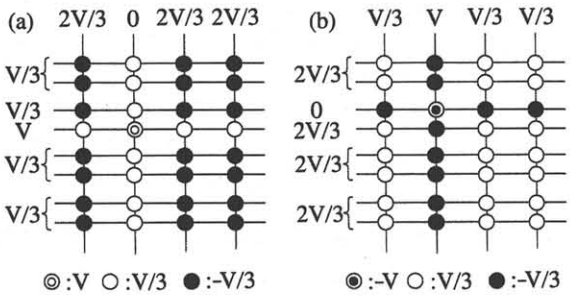

Fig. 4. "Write" operation for a proposed novel array structure. To complete the operation, the first (a) and second (b) pulses are applied successively. Vertical and horizontal lines represent Si stripes and top electrodes of ferroelectric capacitor, respectively.

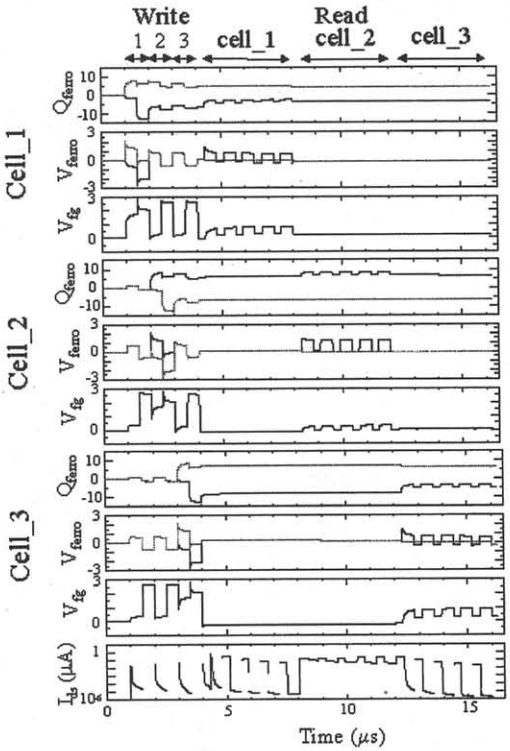

Fig. 6. Simulated waveforms of the write and read operation for a 1×3 array. Black and gray solid lines in Q_{ferro} and V_{ferro} represent terminal A and B, respectively.

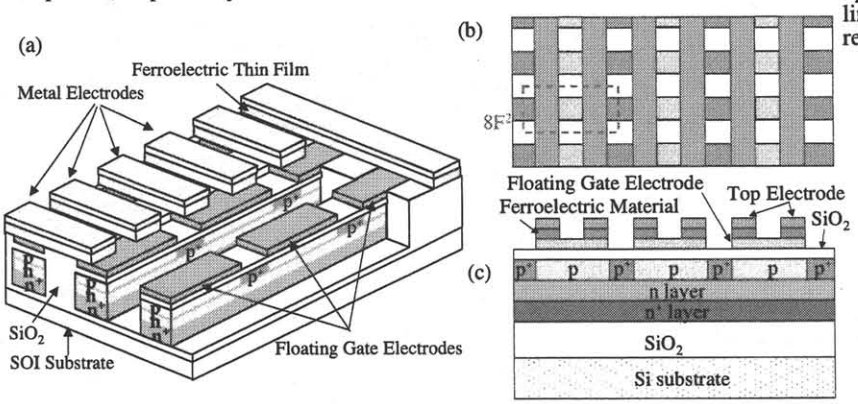

Fig. 5. A proposed planar $8F^2$ cell array. (a) 3 dimensional view, (b) top view and (c) cross section along with a Si stripe.

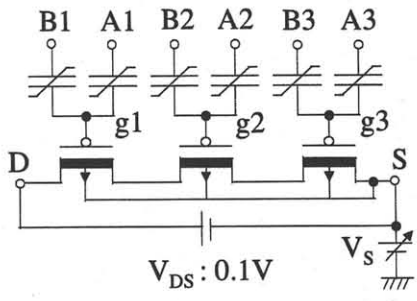

Fig. 7. Schematic of simulated circuit of a 1×3 array.