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Uniformity improvement of SiGe HBT by reduced extrinsic base implanted damage

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1. Introduction

HBT with non-selective SiGe has been promisingly demonstrated for wireless communication. As the emitter window size and the lateral extrinsic/intrinsic base shrink, the defects associated with the extrinsic base implantation will increase extrinsic base resistance ($R_{ext,B}$) and base to collector capacitance (C_{BC}), both of which degrade the device performance and uniformity. In this paper, we used seed layer implantation prior to forming the epi-base with an additional rapid thermal annealing to reduce extrinsic base damage caused by the implantation. In comparison with conventional extrinsic base implant process, devices with a significant improvement of uniformity and yield were achieved.

2. Device Fabrication

A conventional structure of a non-selective SiGe HBT is shown in Fig. 1(a), where the graded $Si_{1-x}Ge_x$ (x=15~0%) layer sandwiched by $Si_{0.85}Ge_{0.15}$ spacer and Si cap layer was epitaxially deposited in a hot-wall UHV/CVD system at 550^{0}C. The pure silane (SiH_4), germane (GeH_4) and diborane (B_2H_6) diluted in He are introduced as the gas source. The detail process can be obtained from our previous report [3]. Fig. 1(b) shows the TEM image of conventional non-selective SiGe HBT. Severe implantation-induced defects are found between the poly emitter and seed layer region (EB). The new approach shown in Fig. 2 has a seed layer implant prior to the SiGe base formation.

3. Device Characterization

Fig. 3 shows the Gummel plot of the transistors made by conventional extrinsic base implantation and the new approach. The transistors have an emitter of 0.6x10 μm^2. An extremely low base-recombination current (I_B) of 0.3 fA and low *2KT* current were obtained from the new approach devices, indicating that few damage-induced defects were created in the extrinsic base region. Histograms of collector current (I_C) under V_{BE} of 0.66V for both extrinsic base implantation and the new approach are shown in Fig. 4. This evaluation was carried out from 29 devices across the 4 inch wafer. Functional devices can be defined for the I_C in the range of 1E-6 to 1E-7 A. The results show that a more uniform I_C distribution and high-yield performance could be obtained with the seed layer implanted samples. The device without the shielding of emitter layer (EB>EO) would be severely damaged by extrinsic base implant. Defects were presumably laterally diffuse into the epi collector region, resulting in the deviation of collector current. Fig. 5 illustrates the current gain versus the rapid thermal annealing temperature after seed layer implantation. RTP temperature at 950^{0}C was found to optimally recover the damage and achieve the highest current gains.

4.Conclusion

We use seed layer implantation prior to forming the epi-base with additional rapid thermal annealing to reduce extrinsic base damage caused by implantation. A significant uniformity improvement of collector current and devices with high-yield performance were achieved

Reference

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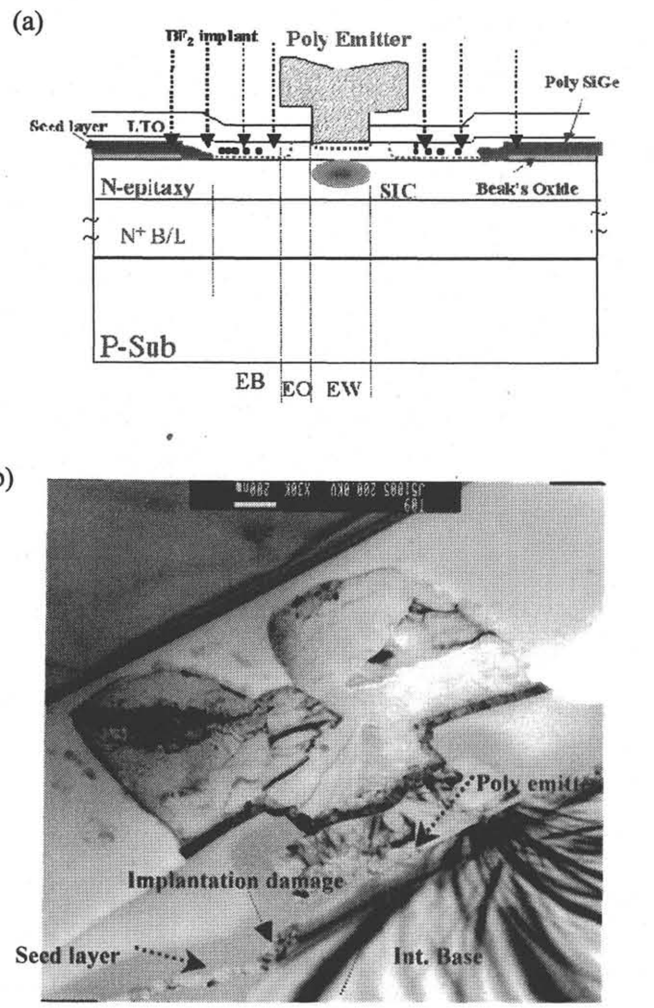

Fig. 1 Schematic (a) and TEM (b) of the non-selective SiGe HBT with extrinsic base implantation

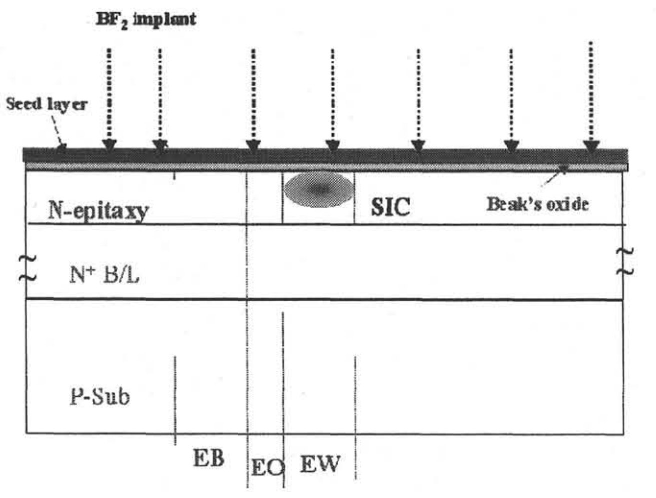

Fig. 2 SiGe HBT with the seed layer implant prior to the formation of epi-base

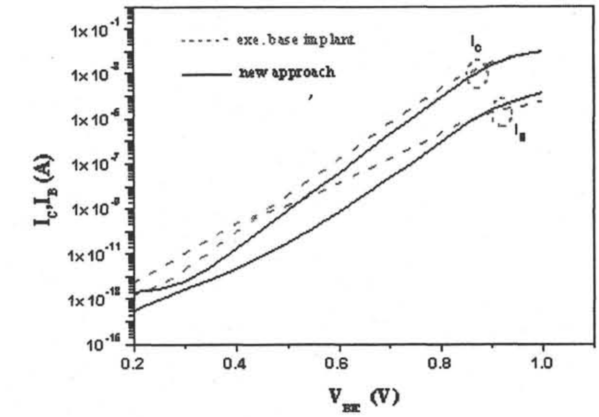

Fig. 3 Forward Gummel plot of SiGe HBT with emitter area of $0.6x10\mu m^2$

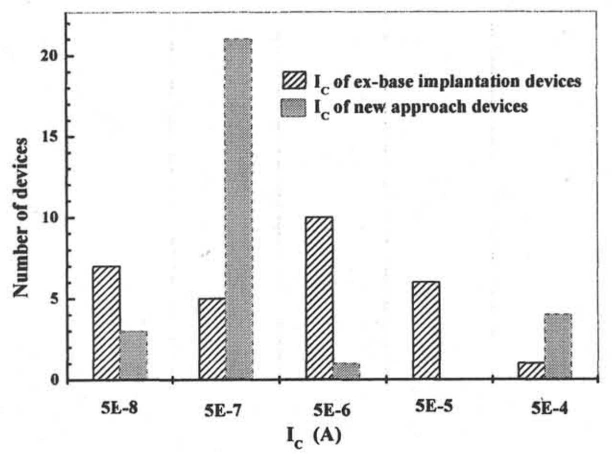

Fig. 4 Histograms of I_C at V_{BE}=0.66V for both extrinsic base and new approach implantation devices

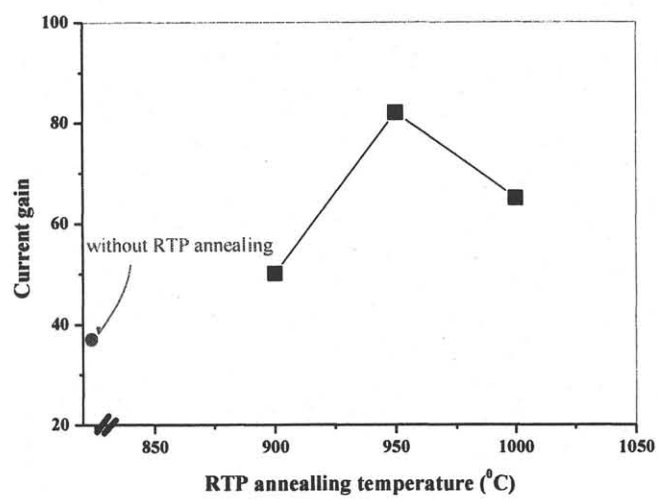

Fig. 5 Current gain of the SiGe HBT versus seed layer RTP annealing temperature