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Effect of AlN Spacer Layer in AlGaN/GaN Heterojunction Field Effect Transistors

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1. Introduction

GaN-based electron devices have many advantages for high temperature and high power operation. Recently, AlGaN/GaN heterojunction field effect transistors (HJFETs) have shown good device performance [1-4].

These characteristics of AlGaN/GaN HJFETs can be improved by using high-quality AlGaN barrier layer. Amano and coworkers have introduced a low-temperature AlN interlayer between the AlGaN layer and the GaN layer at AlGaN/GaN heterostructure grown by metal organic chemical vapor deposition (MOCVD) system [5]. By introducing the AlN interlayer, the strain of the AlGaN layer is erased [6], and the film quality of the AlGaN layer has been improved in the case of high Al-content AlGaN layers.

In this study, we introduced an AlN spacer layer between the AlGaN barrier layer and the GaN channel layer in the conventional HJFET structure. AlGaN/GaN heterostructure films using the AlN spacer layer were grown by radio-frequency plasma-assisted molecular beam epitaxy (rf-MBE), because the optimized growth temperature for GaN, AlGaN and AlN is nearer than that in other growth systems. Therefore, AlGaN/AlN/GaN heterostructure was grown without long growth interruption for varying substrate temperature.

We fabricated the AlGaN/GaN HJFETs using the AlN spacer layer and compared the DC operating characteristics of the HJFETs using the AlN spacer layer with those of the conventional AlGaN/GaN HJFETs, and evaluated the gate Schottky characteristics.

2. Experiment

AlGaN/GaN heterostructure films were grown on sapphire (0001) substrates by rf-MBE. A schematic diagram of the AlGaN/GaN HJFETs is shown in Fig. 1. The device structure of the HJFETs consists of a 200-nm-thick AlN buffer layer, 1.5- μ m-thick GaN layer, 30-nm-thick n-GaN channel layer, 2-nm-thick non-doped spacer layer, 15-nm-thick n⁺-AlGaN barrier layer and 10-nm-thick i-AlGaN cap layer. The n-GaN channel layer and the n⁺-AlGaN barrier layer are doped by Si at a level of $1.0 \times 10^{17} \text{cm}^{-3}$ and $1.0 \times 10^{19} \text{cm}^{-3}$, respectively. In our rf-MBE system, the growth temperature for GaN, AlGaN and AlN

layer is 700, 710 and 730°C, respectively.

We prepared four kinds of HJFET structure films, sample A with Al_{0.25}Ga_{0.75}N layers and AlN spacer layer, sample B with Al_{0.25}Ga_{0.75}N layers and Al_{0.25}Ga_{0.75}N spacer layer, sample C with Al_{0.15}Ga_{0.85}N layers and AlN spacer layer and sample D with Al_{0.15}Ga_{0.85}N layers and Al_{0.15}Ga_{0.85}N spacer layer. The sheet carrier density of each sample was $8.0\text{-}10.0 \times 10^{12} \text{cm}^{-2}$ at room temperature. The electron mobility of sample A, B, C and D were 950, 650, 570 and 450 cm²/(V·s) at room temperature, respectively. Thus, the samples using AlN spacer layer are larger 2DEG mobility than those using AlGaN spacer layer.

The HJFETs were fabricated by the conventional device fabrication process. Mesa isolation was performed by the dry etching with Cl₂ plasma. Ti/Al/Pt/Au ohmic contacts for the source and drain were formed on the AlGaN cap layer and annealed at 830°C for 30sec. The Schottky contact for the gate was formed by Pt/Ti/Au e-beam evaporation. The gate width is 18 μ m, and the gate length is 1.5 μ m in both the device structures.

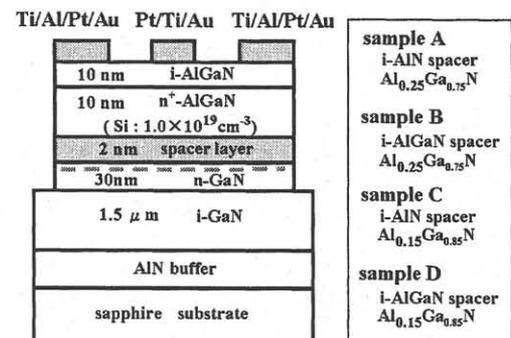


Fig. 1 Schematic diagram of AlGaN/GaN HJFETs.

3. Results and discussion

DC characteristics of these devices were measured at room temperature. Figure 2 shows the drain current-voltage (I_D - V_{DS}) characteristics of the sample A. Maximum transconductance g_{mmax} of sample A is 125mS/mm. Table I shows the device parameter of the each samples. Maximum transconductance of sample B, C and D are 100, 105 and 145mS/mm. In the results of sample A and B, maximum

transconductance g_{mmax} increases by using the AlN spacer layer. In the sample C, low g_{mmax} is caused by poor ohmic contact due to the fabrication process of the sample C.

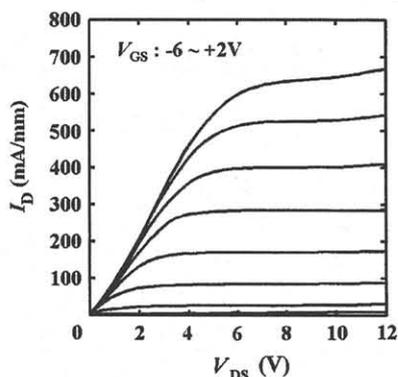


Fig. 2 Drain-source current characteristic I_D of the sample A as a function of drain-source voltage V_{DS} .

Table I Device parameter of each samples

sample	A	B	C	D
spacer	AlN	AlGaIn	AlN	AlGaIn
Al-content of AlGaIn	25%	25%	15%	15%
mobility (cm^2/Vs)	950	650	570	450
g_{mmax}	125	100	105	145
ϕ_b	0.69	0.57	0.55	0.53

In addition, we investigate the gate Schottky characteristics of the samples. Figure 3(a) and (b) show the gate current-voltage (I_G - V_{GS}) characteristics of the sample A and the sample B, respectively. The gate forward current of the sample A is the order of $10^{-1}A$ times smaller than that of the sample B, and the gate reverse current of the sample A is the order of $10^{-3}A$ times smaller than that of the sample B. The saturation current of the sample A, B, C and D are 6.0×10^{-11} , 1.0×10^{-9} , 3.4×10^{-10} and 6.7×10^{-10} , respectively. Therefore, the employment of the AlN spacer layer reduces the gate current of AlGaIn/GaN HJFETs.

The reduction of the gate current shows that the Schottky contact of the gate is improved by the effect of the AlN spacer layer. We analyzed the barrier height ϕ_b of the gate electrode by the following equation:

$$\phi_b = -\frac{kT}{q} \ln \frac{J_s}{A^* \cdot T^2} \quad [eV] \quad (1)$$

where q is the electron charge, J_s is the saturation current density calculated by I_G - V_{GS} characteristics, T is the temperature. A^* is the effective Richardson constant given by $A^* = 2 \pi q m^* k^2 / h^3$, where h is the Plank constant and m^* is the electron effective mass of AlGaIn. The calculated barrier height of the sample A, B, C and D were 0.69, 0.57, 0.55 and 0.53eV, respectively. Therefore, in the case of the AlN spacer layer, the reduction of the gate current is caused by the increase of the Schottky barrier height. It is considered that the Schottky contact is improved by the reduction of the surface state due to the dislocations and the defects.

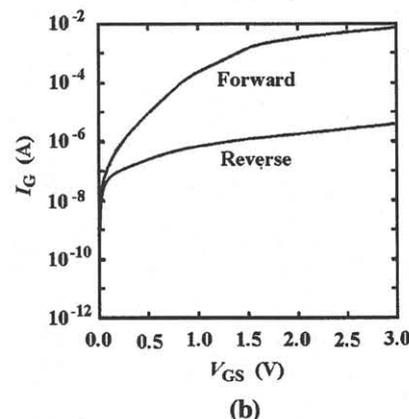
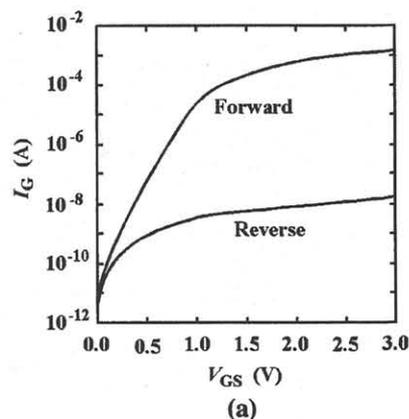


Fig. 3 Gate-source current characteristic I_G of (a) the sample A and (b) the sample B as a function of the gate-source voltage V_{GS} at room temperature.

4. Summary

In summary, AlGaIn/GaN HJFETs using the AlN spacer layer have been demonstrated in DC operation. By using AlN spacer layer, the 2DEG mobility has increased to $950 cm^2/(V \cdot s)$. Moreover, the gate current has been reduced, and the Schottky barrier height has increased. These results have revealed that the employment of the AlN spacer layer improves significantly the DC operating characteristics in AlGaIn/GaN HJFETs.

References

- [1] G. J. Sullivan, M. Y. Chen, J. A. Higgins, J. W. Yang, Q. Chen, R. L. Pierson and B. T. McDermott, IEEE Electron Device Lett. 19, 198 (1998)
- [2] Q. Chen, J. W. Yang, M. Asif Khan, A. T. Ping and I. Aesida, Electron. Lett. 33, 1413 (1997)
- [3] M. Micovic, N.X. Nguyen, P. Janke, W.-S. Wong, P. Hashimoto, L.-M. McCray and C. Nguyen, Electron. Lett. 36, 358 (2000)
- [4] S. T. Sheppard, K. Doverspike, W. L. Pribble, S. T. Allen, J. W. Palmour, L. T. Kehias and T. J. Jenkins, IEEE Electron Device Lett. 20, 161 (1999)
- [5] H. Amano, M. Iwaya, N. Hayashi, T. Kashima, M. Katsuragawa, T. Takeuchi, C. Wetzel and I. Akasaki, MRS Internet J. Nitride Semicond. Res. 4S1, G10.1 (1999)
- [6] H. Amano, M. Iwaya, N. Hayashi, T. Kashima, M. Katsuragawa, I. Akasaki, J. Han, S. Hearne, J. A. Floro, E. Chason and J. Figiel, Jpn. J. Appl. Phys. 37, L1540 (1998)