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P11-5

# A Single-Bias C-Band 29 dBm PHEMT MMIC Power Amplifier

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## 1. Abstract

A C-Band 29 dBm single-bias AlGaAs/InGaAs/GaAs PHEMT MMIC power amplifier for IEEE 802.11a wireless LAN applications is demonstrated. This two-stage amplifier is designed to fully match for a 50 ohm input and output impedance. With only a 8V drain voltage, the amplifier has achieved 22dB small-signal gain, 29.2 dBm 1-dB gain compression power with 25.8% power-added efficiency (PAE) and 30 dBm saturation power with 31% PAE. In addition, high linearity with 39.2 dBm third-order intercept point is achieved to satisfy the stringent linearity demand of OFDM.

## 2. Introduction

High linearity is necessary for Orthogonal Frequency Division Multiplexing (OFDM) which is a proposed multi-carrier modulation technique in the IEEE 802.11a standard for high speed wireless LAN application in the 5 GHz U-NII bands. This technique can provide data rate as high as 54 Mbps and immunity against multipath fading and narrow band interference.

Although GaAs MESFET MMIC power amplifier with 29 dBm saturation output power and good linearity with 41dBm output IP3 has been demonstrated [1], however this MMIC needs dual supply voltages. The other GaAs HBT MMIC power amplifier with similar performance has also been demonstrated [2], and only single supply voltage is used. In general case, depletion mode PHEMT amplifier operates with not only a positive voltage but also another negative voltage for $V_{gs}$, and this is not convenient to system. In this paper, a C-band 29dBm AlGaAs/InGaAs/GaAs depletion mode PHEMT MMIC power amplifier with only single supply voltage is proposed. The measured performance as described later is good and suitable for wireless LAN applications. The chip area of the MMIC as shown in Figure 1 is 2.28 mm x 0.62 mm.

## 3. Circuit Design

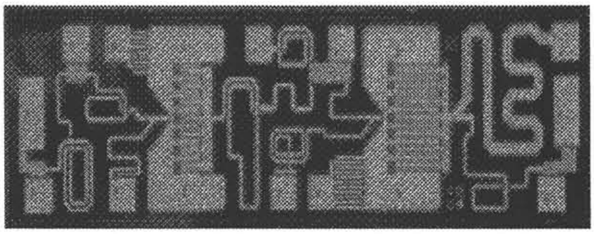

Figure 1 Photograph of C-Band 29dBm self-bias PHEMT MMIC power amplifier

The periphery of the FET for the driver stage is 0.9 mm and the unit gate width is 60 um. The periphery of the power stage FET is 2.4 mm and the unit gate width is 160 um. For single supply voltage purpose, the self bias circuit is used by adding two thin film resistors to the source port of each device.

The first matching network for power amplifier is the output matching which is designed to transfer maximum output power from the FET to the 50 ohm system by Cripps technique [3]. After the output matching network is added, the interstage network is then designed to match the output of the driver stage to the input of the power stage in order to lower the mismatch loss. The lossy match is used by the gate resistor of each stage to improve the stability. Finally, the input network is designed to flatten the small signal gain and improve impedance match for better input return loss. Based on these essential matching networks, an optimization and EM simulation are performed to achieve the required circuit performance.

## 4. Measured Performance

The bias condition for the MMIC is $V_d$ = 8 Volts and $I_{ds}$ = 400 mA including about 100 mA for the driver stage and about 300 mA for the power stage. Under this condition, the small signal gain is 20 to 27 dB from 3.7 to 6.7 GHz. The input return loss is better than 10 dB and the output return loss is about 5.3 to 9 dB from 5 to 6 GHz. Figure 2 shows the measured small signal gain and input/output return loss of the MMIC from 3 to 8 GHz.

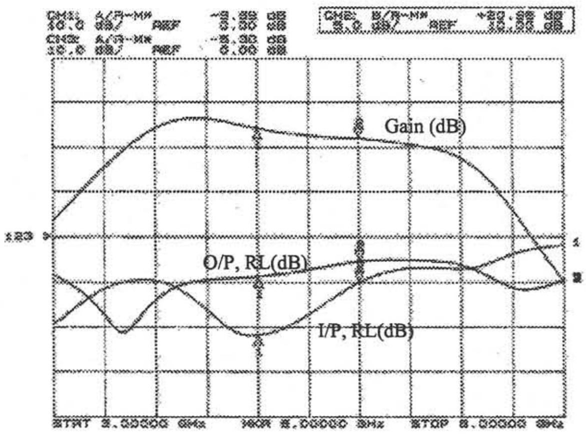


Figure 2 Small signal gain, input and output return loss (dB) versus frequency (GHz)

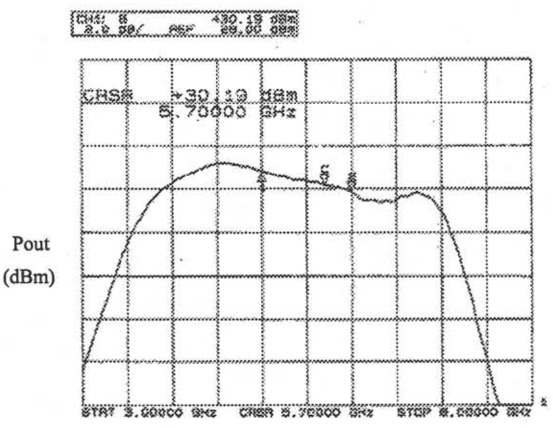


Figure 4 Saturation power versus frequency (GHz)

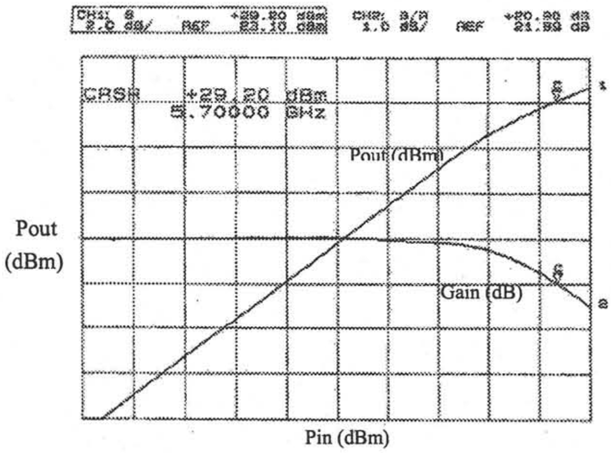


Figure 3 Output power versus input power (dBm)

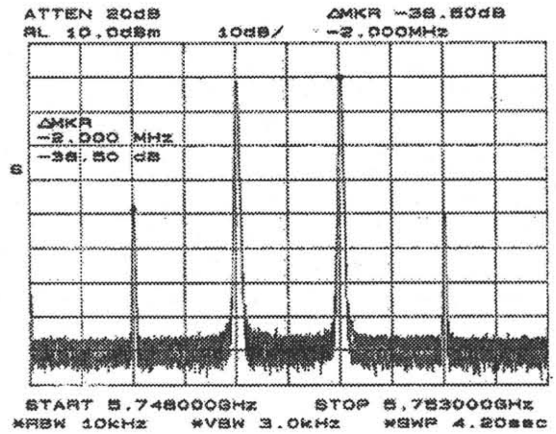


Figure 5 38.5 dBc of 3rd intermodultion distortion @ F1 = 5.75 GHz, F2 = 5.751 GHz

Figure 3 shows the 1-dB gain compression output power of 29.2 dBm with an associated gain of 20.9 dB at 5.7 GHz. The saturation power of 29.5 to 31 dBm from 3.7 to 7.0 GHz is shown in Figure 4 The power added efficiency (PAE) of $P_{1dB}$ and $P_{sat}$ are 25.8% and 31% respectively. The 3rd intermodulation distortion as shown in Figure 5 is 38.5 dBc at 5.75 GHz when two-tone power is 23 dBm. After simple calculation, the IP3 is 39.2 dBm which satisfies high linearity demand of OFDM. These measured results are comparable with other methods previously proposed [1]-[2].

## 5. Conclusions

In summary, a 29 dBm C-band PHEMT MMIC power amplifier with only one positive supply voltage has been developed. Very excellent performance with 29.2 dBm $P_{1dB}$, 25.8% power-added efficiency, 22 dB small-signal gain, better than 12 dB input return loss, and 39.2 dBm third-order intercept point can be achieved.

## Acknowledgments

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