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Low loss and High frequency Interconnection Technology on Membrane supported by Porous Silicon Post

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1. Introduction

As the frequency in integrated circuits is increasing up to several GHz, it is necessary to develop low loss and low cost interconnection technology between chips.

For this application, the thick oxidized porous silicon (OPS) layer on inexpensive CMOS grade wafer shows good performance of -0.15dB/mm loss at 5GHz [1-2]. But, in this case, the signal loss is mainly due to the thick oxide and silicon substrate under the OPS [3]. So, In this experiment, we made signal line on membrane by removing the porous silicon layer instead of oxidizing the layer. And for low loss bonding from pad to pad, porous silicon post bonding pad surrounded by silicon sidewall was developed.

2. Experiments

In figure 1, there is a schematic diagram of MCM (Multi-Chip Module) packaging technology using CPWs on membrane and porous silicon post.

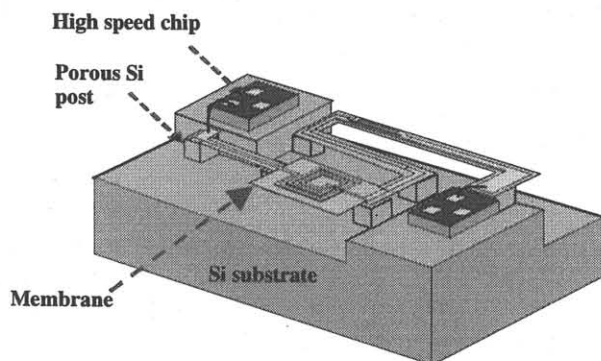


Fig. 1 Schematic diagram of MCM packaging technology using CPWs on membrane supported porous silicon post.

Figure 2 shows schematic diagram of CPW on membrane and cross sectional view of coplanar waveguide on membrane supported by silicon post and the variables for fitting signal line to 50Ω impedance, where W is signal line width, G is ground line width, S is spacing between signal and ground line.

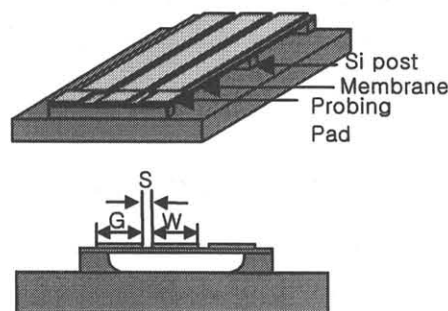


Fig. 2 Schematic diagram of CPW on membrane and cross sectional view.

The Porous silicon layer was fabricated by anodization process on $\langle 100 \rangle$ boron doped silicon substrate of $8-12\Omega\text{ cm}$ resistivity [1]. Before anodizing the silicon substrate, there was a Si_3N_4 mask layer patterned for silicon posts and the mask layer was grown to 5300\AA at 780°C with LPCVD. In the anodization process, the current density is 20mA/cm^2 , and the thickness of porous silicon layer is $40\mu\text{m}$. After the selectively porous silicon layer is prepared, the dielectric layers for membrane was deposited with RPCVD. At first, 2000\AA thick SiO_2 layer is grown with SiH_4 , N_2O and He at 200°C , and after that 2000\AA SiN_x layer is deposited with SiH_4 , NH_3 and He at 200°C , and finally, SiO_2 layer is raised to 2000\AA under the same condition as that of the first layer.

Coplanar waveguide is formed by conventional monolithic microwave integrated circuit (MMIC) process, such as lithography, metal evaporation, lift-off and Au plating. After that, the membrane dielectric under the coplanar waveguide is patterned by RIE with CF_4 and O_2 for NaOH solution to intrude through the open area and etch porous silicon sacrificial layer rapidly. Finally, the porous silicon sacrificial layer is etched in 0.25% NaOH solution for 2hours without any protection mask for metals, and the etching rate is higher than $2.5\mu\text{m/min}$.

3. Results

Figure 3 shows photograph of the middle part of the fabricated coplanar waveguide, where the dimension is $W = 150\mu\text{m}$, $G = 100\mu\text{m}$, $S = 10\mu\text{m}$ and the total length is 5mm.

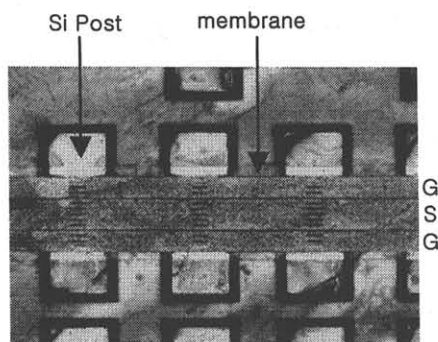


Fig. 3 Photograph of the middle part of the fabricated CPW.

In figure 4, there are maximum available gains of the CPWs, one has silicon post and the other has porous silicon post for probing pad. CPW having pad on silicon post was measured to 15GHz, it displays -1.2dB/mm loss at 15GHz, on the other hand, CPW on porous silicon post shows -0.4dB/mm loss at 15GHz before releasing the membrane by etching the porous silicon layer, and -0.15dB/mm loss at the same frequency after etching the porous silicon layer.

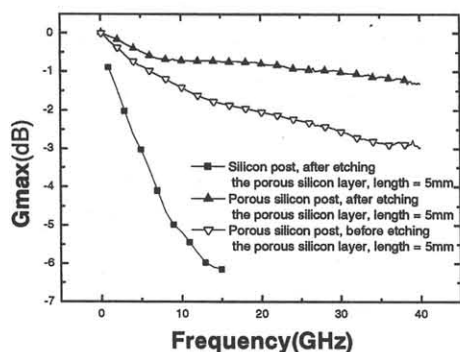


Fig. 4 Measured maximum available gains of CPWs with probing pad supported on porous silicon post and silicon post

And figure 5 shows return losses of the three types of CPWs.

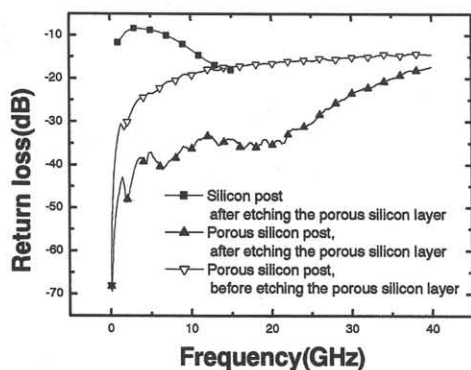


Fig. 5 Measured Return loss of CPWs

Figure 6 displays the cross section of porous silicon post surrounded by silicon sidewall, cut along to length direction, and it has sufficient robustness for wire bonding.

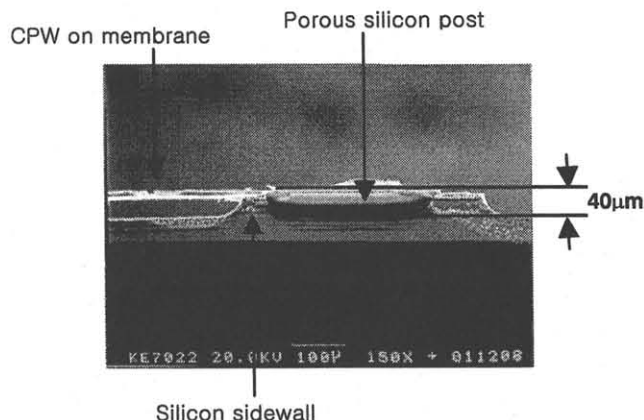


Fig. 6 SEM picture of the cross section of porous silicon post surrounded by silicon sidewall.

4. Conclusions

In this experiment, the coplanar waveguide on the membrane utilizing porous silicon as a sacrificial layer showed much improved transmission performance (from -0.4dB/mm loss to -0.15dB/mm loss at 15GHz) by removing the porous silicon layer. And, by adopting the porous silicon post for probing and bonding, we decreased signal loss from -1.2dB/mm , in the case of silicon post, to -0.15dB/mm at 15GHz. The signal loss will be more decreased by increasing the etching depth and this multi-chip packaging technology is of promise for high frequency and high power chip integration.

References

- [1] C. M. Nam, and Y. S. Kwon, "Coplanar waveguides on silicon substrate with thick oxidized porous silicon (OPS) layer" IEEE Microwave and Guided Wave Lett., vol. 8, no. 11, pp. 369-371, Nov., 1998.
- [2] C. M. Nam and Y. S. Kwon, "SOPS substrate for microwave power chip-packaging," in IEEE 5th Topical Meeting Electrical Performance of Electronic Packaging, PP. 202-204, Oct., 1996.
- [3] R. L. Peterson and R. F. Drayton, "Dielectric properties of oxidized porous silicon in a low resistivity substrate," IEEE MTT-S International Microwave Symposium Digest, vol.2, pp. 767-770, 2001.