Low-leakage 0.11 μm CMOS for Low-Power RF-ICs and SRAMs Applications


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1. Introduction
In this paper, we demonstrate optimized low-leakage (LL) 0.11 μm CMOS with 193 nm lithography and Cu/low-k for low-power (LP) RF-ICs and SRAMs applications. For 1 pA/μm nominal off-state current (I_L) @1.1V_{CC}=1.65V, n/pMOS with excellent 520/210 μA/μm nominal drive currents @V_{CC}=1.5V were achieved. Very good cut-off frequency (f_T) and maximum-oscillation frequency (f_{max}) of 43 GHz and 35 GHz, respectively, were attained for 0.11 μm nMOS at maximum transconductance (g_m). This result show that this 0.11 μm nMOS is very suitable for S-band and C-band low-power RF-IC applications. Process capability for low power applications is demonstrated by using a CMOS 6T-SRAM with 2.43 μm² cell size. Measured standby current (I_{SB}) is 3.6 pA/cell @V_{CC} for SRAMs at RT. In addition, channel, LDD and pocket implants are also fine-tuned for ultra-low-power (ULP) SRAMs applications, ultra-low I_{SB} of 0.42 pA/cell and 2.25 pA/cell measured at RT and 85°C, respectively.

2. Results and Discussions
Fig. 1(a) shows a cross-sectional poly-gate TEM of a 0.11 μm nMOS. As shown in Fig. 1(b)-(c) and Fig. 2(a), we can observe that the I_{SB} versus I_{off} characteristic of optimized 0.11 μm LL transistors, either in pMOS or nMOS, is N-shaped because strong reverse-short-channel-effect (RSCE) needs to be adopted to maximize device’s window [1], [2]. In addition, maximum process window is shown if nominal n/pMOS is designed around the lowest point of the I_{SB} vs. I_{off} curve. Channel, LDD and pocket implants of the LL n/pMOS are also fine-tuned to generate another set ultra-low-leakage (ULL) n/pMOS for ULP SRAMs applications. Fig. 2(b) compares the sub-threshold behavior for 0.11 μm LL and ULL n/pMOS. This figure exemplifies the varying degrees of devices’ I_{off}, I_{SDL}, and I_{BTBT} leakage control required by 0.11 μm LL/ULL transistors with different V_{CC} and I_{off} specifications. As can be seen, nominal I_{off}’s of LL and ULL n/pMOS are about 1.8 pA/μm and 0.3 pA/μm, respectively. As shown in Fig. 2(c), excellent f_T and f_{max} of 43 GHz and 35 GHz, respectively, were achieved for 0.11 μm nMOS at maximum g_m. This result shows that this 0.11 μm nMOS is also very suitable for S-band and C-band low-power RF-ICs applications.

Fig. 3(a) shows SEM top view of an embedded 6T SRAM cell using 193 nm lithography with binary mask. Fig. 3(b) shows the measured I_{SB} vs. V_{CC} of a LP SRAM cell (cell size 2.43 μm²) with boron cell implants (6.0x10^{12} cm⁻²) and (1.2x10^{13} cm⁻²). Implant energies are both equal to 25 keV. We can observe that SRAM with higher boron cell implant exhibits higher I_{SB} at RT and lower I_{SB} at high temperature (85°C and 125°C). The reason is that SRAM with higher boron cell implant exhibits larger temperature-insensitive I_{SDL} and smaller temperature-sensitive I_{BTBT}. In addition, we observe that the optimum I_{cell} which minimizes I_{SB} of a SRAM cell is a function of temperature (not shown here).

Fig. 2(c) shows the leakage components and directions of a SRAM cell under standby bias condition. As we can see in Fig. 2(c), the total leakage of a SRAM cell includes I_{off} of PD-1, PU-1 and PG-1 transistors, I_{off} of PD-2 and PU-2 transistors, and accumulation mode gate leakage I_{G} of PG-2 transistor. Table I shows the six individually measured leakage components of a ULP SRAM cell with 2.43 μm² cell size. As we can see clearly, the projected I_{SB} of a SRAM cell (0.596 pA/cell @RT and 2.163 pA/cell @85°C) is very close to the measured I_{SB} data (0.42 pA/cell @RT and 2.25 pA/cell @85°C). This means the analytical approach of SRAM standby leakage is reliable. Under normal condition of operation, i.e. about 85°C, the summation of total gate leakage (0.251 pA/cell) is lower than that of total I_{off} (1.91 pA/cell). However, the summation of total gate leakage (0.225 pA/cell) is already a little higher than that of total I_{off} at RT (0.17 pA/cell).

3. Conclusions
In conclusion, first, we observe that the I_{SB} versus I_{off} characteristic of optimized 0.11 μm LL/ULL n/pMOS is N-shaped. Maximum process window is exhibited if nominal n/pMOS is designed around the lowest point of the I_{SB} vs. I_{off} curve. Secondly, Very good f_T and f_{max} performance were achieved for 0.11 μm nMOS at maximum g_m, which means this 0.11 μm nMOS is also very suitable for S-band and C-band low-power RF-ICs applications. Finally, The projected I_{SB} of a SRAM cell by summing its six leakage components either at room temperature or at high temperature is very close to the measured I_{SB} data. This means the analytical approach of SRAM standby leakage is reliable.

Acknowledgement
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References
Fig. 1(a) A cross-sectional poly-silicon gate TEM of a 0.11 µm LL nMOS.
Fig. 1(b) A measured and a simulated N-shaped $I_{\text{on}}$ vs. $I_{\text{off}}$ curves of optimized 0.11 µm LL pMOS.
Fig. 1(c) Comparisons between $I_{\text{on}}$ vs. $I_{\text{on}}$ curves of optimized 0.11 µm LL pMOS and other conditions.

Fig. 2(a) Comparisons between $I_{\text{on}}$ vs. $I_{\text{off}}$ curves of optimized 0.11 µm LL nMOS and other conditions.
Fig. 2(b) Sub-threshold ($I_{\text{on}}$ vs. $V_{\text{gs}}$) characteristics of 0.11 µm LL and ULL n/pMOS.
Fig. 2(c) Microwave characteristics of 0.11 µm LL nMOS at maximum transconductance ($g_{m}$).

Fig. 3(a) SEM top view of an embedded 6-T SRAM cell using 193 nm lithography with binary mask.
Fig. 3(b) The measured $I_{\text{on}}$ vs. $V_{\text{cc}}$ characteristics of 0.11 µm LL SRAM.
Fig. 3(c) Schematic plot of the six leakage components of a SRAM cell.

Table I  Summary of various leakage components of a ULP SRAM with cell size 2.43 µm².

<table>
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<tr>
<th>Dim (µm²)</th>
<th>PG (pA/µA)</th>
<th>PD (pA/µA)</th>
<th>PU (pA/µA)</th>
<th>$I_{\text{on}}$ (pA/cell) (PG+PD+PU)</th>
<th>$I_{\text{on}}$ (pA/cell) (PD+PU (inv.) + PG (acc.))</th>
<th>$I_{\text{on}}$ (pA/cell) (PG+PD+PU)</th>
<th>$I_{\text{off}}$ (pA/cell)</th>
<th>Measured $I_{\text{on}}$ (pA/cell)</th>
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<tr>
<td></td>
<td>0.180.22</td>
<td>0.2550.16</td>
<td>0.180.18</td>
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<td>25</td>
<td>0.058</td>
<td>0.097</td>
<td>0.016</td>
<td>0.17</td>
<td>0.324</td>
<td>0.405</td>
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<td>85</td>
<td>0.88</td>
<td>0.73</td>
<td>0.30</td>
<td>1.91</td>
<td>0.362</td>
<td>2.274</td>
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<td>Ioff ratio</td>
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<td>7.47</td>
<td>18.94</td>
<td>11.18</td>
<td>1.12</td>
<td>4.69</td>
<td>4.67</td>
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<tr>
<td>85C/25C</td>
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