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Novel Vertical Polysilicon Thin-Film Transistor with Excimer-Laser Annealing

Ming-Zhen Lee, Chung-Len Lee, Tan-Fu Lei

Department of Electronic Engineering National Chiao Tung University, Hsinchu, Taiwan, R. O. C.
Phone: +886-3-5712121 ext 54219 Fax: +886-3-5724361 E-mail: mzlee.ee85g@nctu.edu.tw

1. Introduction

Vertical thin film transistors (VTFTs) are suitable for high-density integration since their channel lengths are determined by the thickness of SiO_2 or polysilicon films instead of the photolithographic limitation. Much work had been devoted to developing and studying VTFTs [1][2]. The lateral diffusion of dopants in a short channel device is a serious problem that increases the off-stat leakage current. The leakage current can be reduced by the drain engineering [3][4]. Here, we propose a novel VTFT structure with excimer laser annealing (ELA), but without self-alignment problem. The ELA on source and drain decreases the process temperature, suppresses the lateral diffusion of dopants in short channel devices and increases the driving current.

2. Experiment

The key process sequence of the proposed VTFT is shown in Fig. 1. A 100-nm thick α-Si:H layer, a 300-nm thick TEOS oxide, a 100-nm thick α-Si:H layer and a 300-nm thick TEOS oxide are deposited subsequently on an oxidized wafer as source, isolated oxide I, drain and isolated oxide II by PECVD. Both source and drain layers are doped with PH_3 plasma at 300 ℃ by PECVD and activated by ELA to reduce series resistance. Then these films are patterned to form a vertical edge. A 100-nm polysilicon is deposited on the step by LPCVD to form channel layer. Then a 100-nm PECVD TEOS oxide and a 100-nm sputtered TiN layer are deposited subsequently as gate oxide and gate. Then these three films are etched to define gate patterns. A 300-nm thick PECVD TEOS is deposited and etched to define contact hole. Finally, a 500-nm Al is deposited and patterned for gate/source/drain metal. A plasma treatment is performed by pure NH3 plasma at 300 ℃ for 30 min in PECVD.

3. Results and discussion

Fig. 2 presents a TEM image of a VTFT with the deposition of as-deposited polysilicon channel layer. The α-Si:H layers for source and drain are activated and crystallized by ELA. The sheet resistance is 110 Ω/□. The grain size of the as-deposited polysilicon layer is small in the vertical region of the channel. Fig. 3 presents a SEM image of a VTFT after TiN gate deposition. The thickness of the gate oxide in the vertical region is 50nm although a 100-nm thick TEOS oxide is deposited on the device. The step coverage of gate oxide and sputtered TiN film is good in the vertical region. Fig. 4 shows the ID-VG curves of VTFTs with or without NH_3 plasma treatment. The channel width/length of VTFTs is 10μm/0.3μm. The threshold voltage and mobility of the polysilicon VTFT without plasma treatment are 5.1V and 21 cm^2/V-sec. After NH_3 plasma treatment, the threshold voltage is reduced to 2.3V and the mobility increases to 48 cm^2/V-sec. The mobility of VTFT is high for an as-deposited polysilicon channel without any crystallization treatments. The successive ID-VG curves and high on/off current ratio show that the low temperature process and ELA have suppressed the lateral diffusion of dopants from source and drain into channel. Moreover, the ELA effectively reduces the series resistances of source and drain layer at low temperature to increase the driving current. Fig. 5 shows the ID-VD curves of a VTFT with 30min NH_3 plasma treatment. The carrier drift velocity has been saturated because of the short channel effect. Fig. 6 shows the leakage current of gate oxide on VTFT. The gate oxide in vertical region has very low leakage current because of the deposition of gate oxide on undoped polysilicon layer.

4. Conclusions

In this paper, we investigated a novel VTFT structure with ELA. There is no self-alignment problem in this

structure. The ELA actives the dopants, reduces the series resistance of source/drain layers under low temperature, and then yields a high quality polysilicon VTFT.

Acknowledgment

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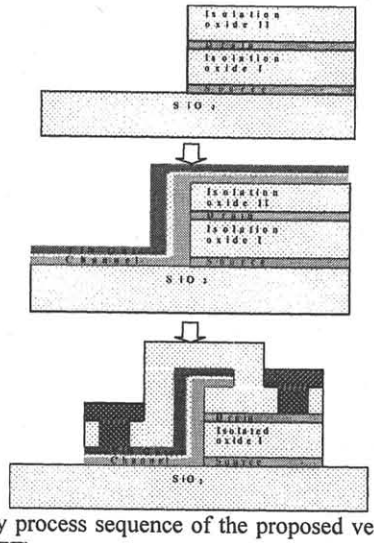

Fig. 1 The key process sequence of the proposed vertical thin-film transistor (VTFT)

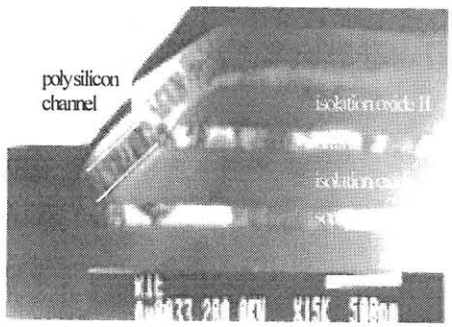

Fig. 2 TEM image of a VTFT after the deposition of polysilicon channel layer. The α -Si:H layers for source and drain are crystallized by ELA. The grain size of the as-deposited polysilicon layer is small in the vertical region of the channel.

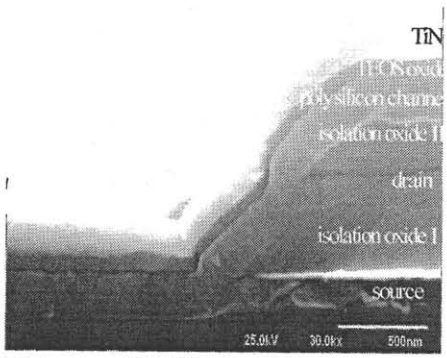

Fig. 3 SEM image of VTFT after TiN gate deposition The step coverage of gate oxide and sputtered TiN film is good in the vertical region.

References

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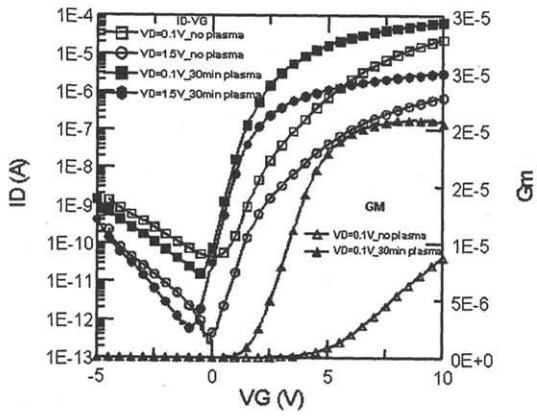

Fig. 4 The ID-VG curves of VTFTs with or without NH_3 plasma treatment. The channel width/length is 10μm/0.3μm. Polysilicon VTFT with NH_3 plasma treatment has a movility of 48 cm^2/V-sec.

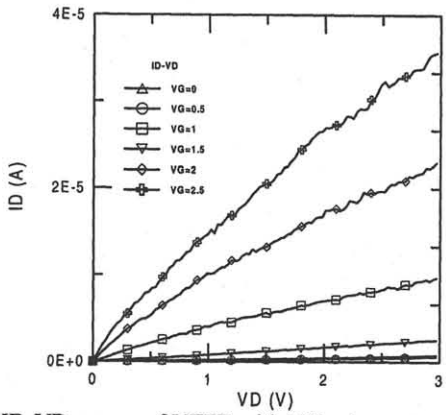

Fig. 5 The ID-VD curves of VTFT with NH_3 plasma treatment. The carrier drift velocity has been saturated because of the short channel effect.

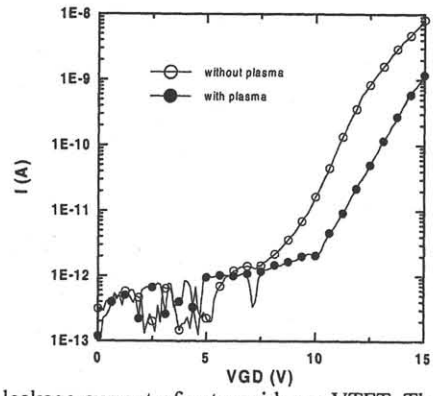

Fig. 6 The leakage current of gate oxide on VTFT. The gate oxide in the vertical region has a very low leakage current because of the deposition of gate oxide on undoped polysilicon layer.