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# Excellent Ambipolar Characteristics on Schottky Barrier Thin-Film Transistors with Excimer Laser Annealing Treatment

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## 1.Introduction

Recently we have proposed and demonstrated a novel Schottky barrier (SB) poly-Si TFT with field-induced-drain (FID) extension [1]-[5]. Our experimental results indicate that such device is capable of ambipolar operation and does not suffer from GIDL-like off-state leakage current [1]-[5]. Poly-Si films prepared using solid-phase crystallization (SPC) technique were employed as the active channel layers in our previous study. Such materials, however, are known to suffer from the small grain size as well as large amount of defects both at grain boundaries and inside the grains. In this work, in order to further enhance the device performance, we fabricated and characterized FID SB TFTs having poly-Si channel layers prepared by excimer laser annealing (ELA).

## 2.Device Structure and Operation

Figure 1 shows the cross-sectional view of the SB TFT with FID structure. Detailed fabrication flow could be found in our previous reports [3][4]. In this study, the 50nm-thick active channel layer is made up of re-crystallized poly-Si layer by ELA method. ELA was performed by irradiating the amorphous Si layer with energy density of 250mJ/cm$^2$ for 100 shots. Gate oxide (100 nm) and passivation oxide (400 nm) were deposited using PECVD. Co silicide serving as the metallic source/drain of the SB TFTs was formed using slef-aligned silicidation (salicide) method.

During device operation, a proper fixed bias is applied to the sub-gate to form electrical junction in the offset channel region. Depending on the polarity of the sub-gate-bias, the device can be set for either n- or p-channel operation.

## 3.Results and Discussion

Figure 2 shows the subthreshold characteristics of a device with ELA poly-Si channel layer. Excellent device performance in terms of steep subthreshold slope and high on/off current higher than $10^8$ for both p- and n-channel operation are demonstrated, for the first time, on a Poly-Si TFT device. The results are much better that those on SPC poly-Si channel we reported previously [1]~[5], indicating that the ELA is very effective in enhancing the performance of SB TFTs.

It has been shown that the applied sub-gate bias tends to increase the on-state current [3]. This is ascribed to the fact that the sub-gate bias could modulate the tunneling distance of source-side Schottky junction during on-state operation and thus the on-state current. Figure 3 depicts the effects of sub-gate bias on the p- and n-channel operations of the fabricated device. It is found that the major improvement appears on the on-state current of n-channel operation. This is reasonable since the barrier height for electrons is larger than for holes [6], and thus the modulation of tunneling distance of the source-side Schottky junction has a larger impact on the n-channel operation. Figs. 4 and 5 show $I_D$-$V_G$ characteristics versus channel length and FID length ($X_D$), respectively. In the two cases, the p-channel operation shows stronger dependence on the structural parameters. This again indicates that the source-side tunneling process is more dominant for n-channel operation.

Note that the $I_D$-$V_G$ curves for p-channel operations shown in Figs.2 ~ 5 depict two different slopes in the subthreshold region. This phenomenon is not clear at this stage and might be related to the nature of the ELA poly-Si layers used in this work.

## 4. Conclusions

SBTFT devices with ELA poly-Si active channel were successfully fabricated in this work. Excellent device performance in terms of steep subthreshold slope and high on/off current higher than $10^8$ for both p- and n-channel operation are demonstrated, for the first time, on a single poly-Si TFT device. Source-side tunneling process is found to be important for device operation, especially for the n-channel operation that has a larger barrier height. The stellar performance with on/off current ratio larger than $10^8$ for both n- and p-channel modes of operation, together with its inherent ambipolar capability, implantless process, silicided source/drain, low thermal budget, and simplified CMOS integration scheme, makes this kind of device a promising candidate for future AMLCDs and SOP applications.

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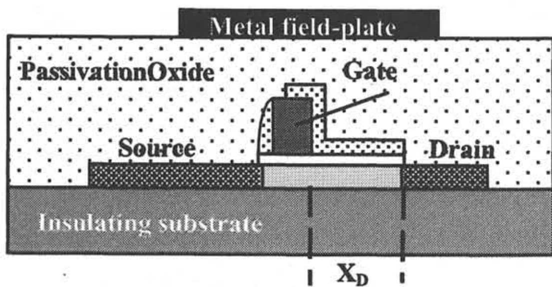



Fig.1 Structures of SBTFT device with FID. $X_D$ is the length of FID.

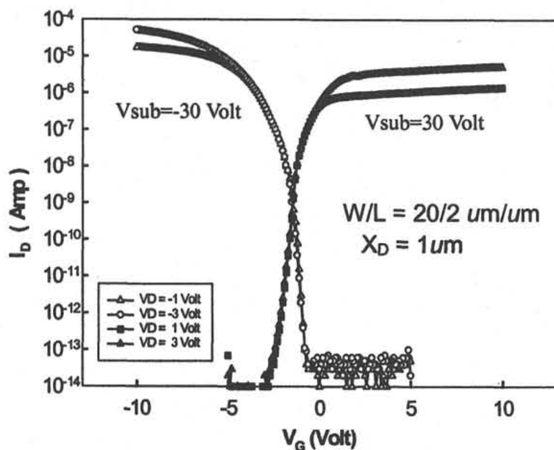
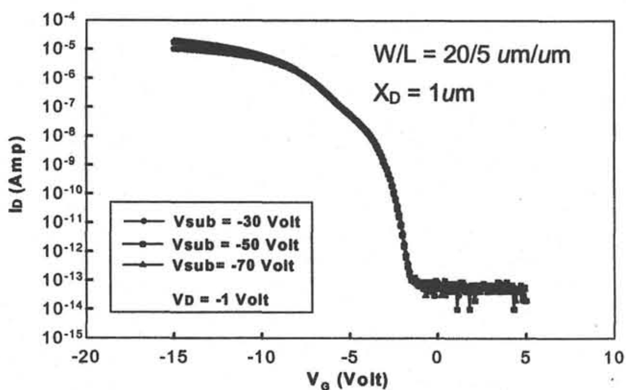



Fig.2 $I_D$-$V_G$ characteristics for *p*- (empty symbol) and *n*- (filled symbol) channel operation of SBTFT with FID. FID structure.



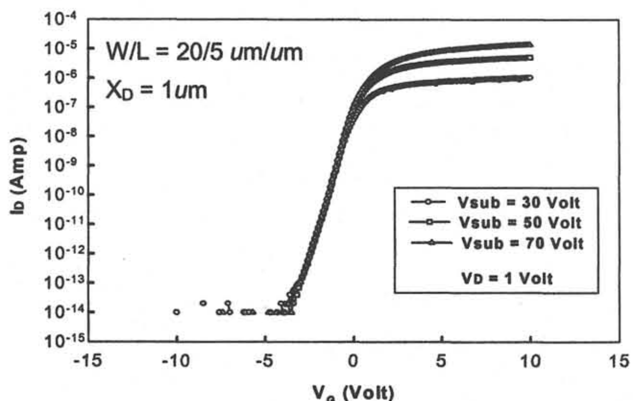
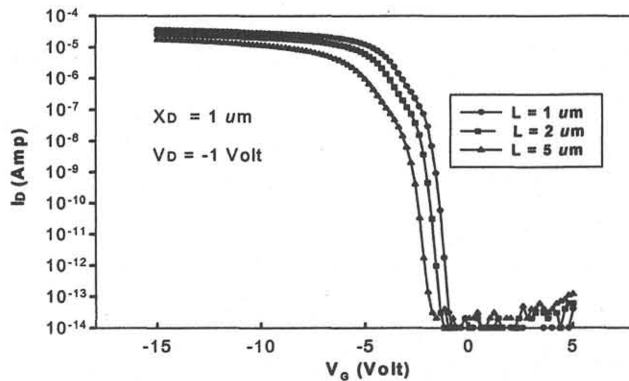




Fig.3 $I_D$-$V_G$ characteristics with different sub-gate bias for *p*- (top) and *n*- (bottom) channel operation.



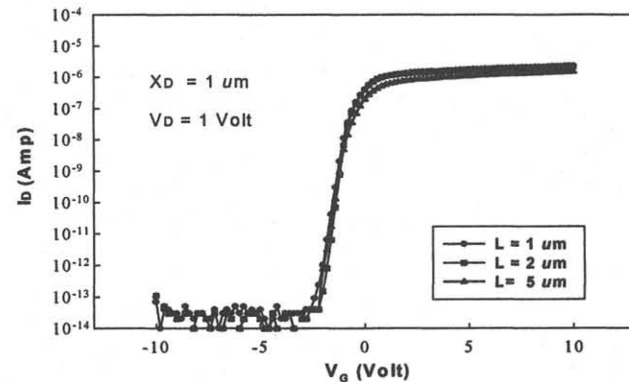
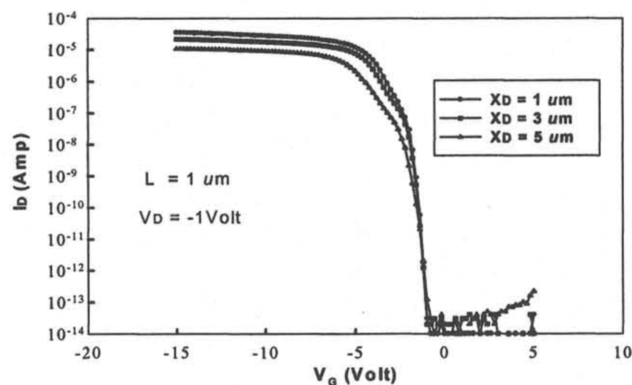




Fig.4 $I_D$-$V_G$ with different channel length for *p*- (top) and *n*- (bottom) channel operation.



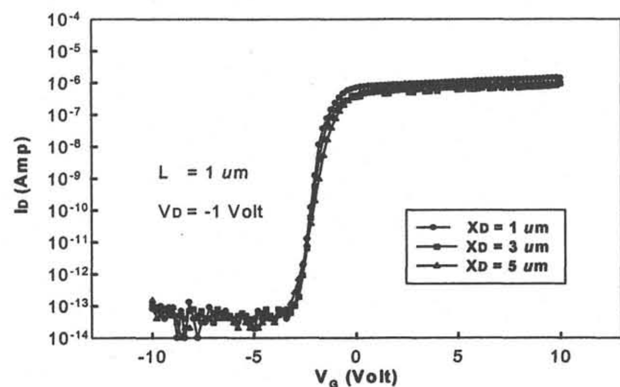




Fig.5 $I_D$-$V_G$ with different FID length for *p*- (top) and *n*- (bottom) channel operation.