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1.0V High Performance Device with Reduced Parasitic Junction Capacitance and Suppressed Junction Leakage Current for 0.1μm Technology

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1. Introduction

High speed CMOS requires both high drive current and low parasitic capacitance while the low power CMOS needs a low standby leakage current. To satisfy these requirements, we need to reduce the parasitic junction capacitance (Cj) and suppress the junction leakage current (Ileak,j) as optimizing high performance MOSFETs [1]. However, the device degradation can occur by inserting an additional process to reduce the parasitic Cj and Ileak,j. In this paper, high performance devices beyond 0.1μm technology are demonstrated to improve the ring oscillator (RO) delay with the reduced Cj and Ileak,j through a careful tailoring of the channel doping profile, the pocket implantation and graded S/D implantation.

2. Experimental

Dual gate 0.1μm CMOS with 70nm physical gate length and equivalent oxide thickness (EOT) 1.7nm is implemented with shallow trench isolation 4kÅ as shown in Fig. 1. Channel for NMOS and PMOS was doped by using boron dose of $2\text{-}6\times10^{12}/cm^2$ with energies varying from 10 to 40keV and by using arsenic dose of $2\text{-}6\times10^{12}/cm^2$ with energies varying from 100 to 200keV respectively. Gate dielectric oxide was grown by using NO gas and gate poly electrode was formed subsequently. An offset spacer for reducing the gate to source/drain (S/D) overlap capacitance (Cgdo) was followed by a shallow S/D extension (SDE) with the abrupt pocket implantation. After forming L-shaped spacer, N+S/D implantation was done with arsenic dose of $3\times10^{15}/cm^2$ at 40keV followed by phosphorus dose of $1\text{-}5\times10^{13}/cm^2$ at energies varying from 30 to 60keV for a graded N+S/D junction. Similarly, boron P+S/D implantation was used with a dose of $3\times10^{15}/cm^2$ at 4keV and then boron was implanted with a dose of $1\text{-}5\times10^{13}/cm^2$ at energies varying from 10 to 15keV for a graded P+S/D junction. After S/D activation of 1050°C spike rapid thermal annealing (RTA) with cover SiO_2, $CoSi_2$ was formed on deep S/D and gate electrode.

3. Results and discussion

The parasitic Cj and Ileak,j can be suppressed by the optimization of the channel, pocket, S/D and graded S/D doping profile. As shown in Fig. 2, the simulation result shows that n-channel boron energy of 10keV is feasible for reducing the area/periphery Cj and Ileak,j. In Fig. 3, channel energy condition of 10keV reduces N+/PW area junction capacitance (Cja) by 70% compared to 40keV condition after junction side-wall capacitance (Cjsw) is decoupled separately. Fig. 4 shows the reduced P+/NW Cja by 80% after Cjsw effect was decoupled as we optimized the doping profile with lower channel energy, higher pocket tilt and additional P+S/D graded implantation. Fig. 5 shows more reduction of N+/PW Cja with the fine tuning for N+S/D graded implantation condition. In this work, the parasitic capacitances were significantly reduced compared to the relevant published data [2] as shown in Table I. Careful doping profile optimization results in a reduction of N+/PW Cja to $0.8fF/\mu m^2$ and P+/NW Cja to $0.7fF/\mu m^2$. Furthermore, Cgdo and the side wall junction capacitance under gate electrode (Cjswg) are minimized with the optimized SDE and pocket implantation condition.

In the same way as the parasitic capacitance reduction, N+/PW and P+/NW Ileak,j was suppressed to $<50nA/cm^2$ for area type diode (area=$6600\mu m^2$, perimeter=460μm) and to <0.1fA/μm for periphery type diode (area=$12000\mu m^2$, perimeter=64800μm) by the optimization of channel doping, deep S/D and S/D graded implantation as shown in Fig. 6 and Fig. 7 respectively [3][4].

High performance devices were achieved by the abrupt pocket profile, shallow SDE junction [5] and spike RTA as shown in Fig. 8. Optimized SDE and pocket structure not only minimized the parasitic series resistance to improve the driving current but also reduced Cgdo to decrease the parasitic loading capacitance [6]. The propagation delay with 16.3% lower N+/PW Cja is 6.5% faster than the higher Cja condition at the same driving current and the bigger gate length shows slower RO delay as shown in Fig. 9. The unloaded ring oscillator achieved 13ps/stage delay with the realized low parasitic capacitance and the high performance devices at 1.0V operation.

4. Conclusions

For 0.1μm technology, high performance CMOS device was demonstrated with a superior drive current. Careful optimization in channel, pocket and source/drain doping profile results in a reduction of N+/PW and P+NW area junction capacitance to $0.8fF/\mu m^2$ and to $0.7fF/\mu m^2$ respectively. In addition, area diode leakage current $<50nA/cm^2$ and periphery diode leakage current <0.1fA/μm are achieved. The reduced parasitic capacitance and the high driving current of NMOS 625μA/μm and PMOS 285μA/μm at off-state current 15nA/μm enable to operate the unloaded ring oscillator with 13ps/stage delay at 1.0V operation.

References

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Table I Parasitic junction capacitances

CMOS Logic	NMOS	PMOS
Cj [fF/μm^2]	0.8	0.7
Cjsw [fF/μm]	0.03	0.03
Cjswg [fF/μm]	0.4	0.3
Cgdo [fF/μm]	0.2	0.3

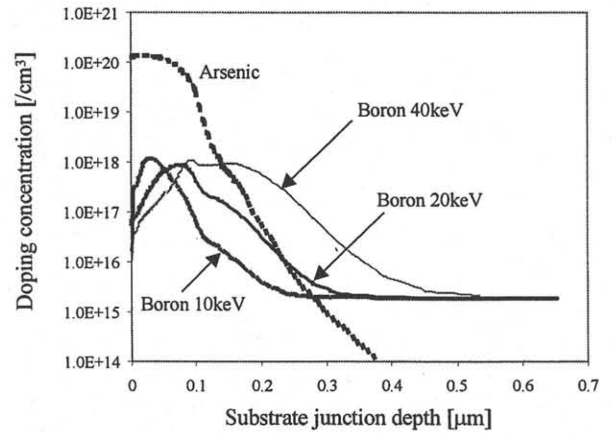

Fig. 2 Simulation doping profile of boron n-channel region with varying implantation energy

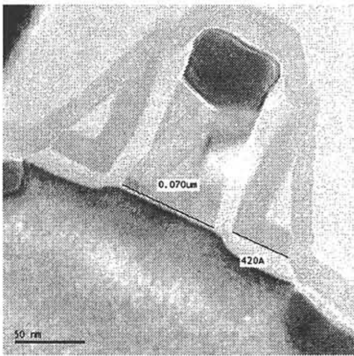

Fig. 1 TEM micrograph with gate length 70nm and EOT 1.7nm

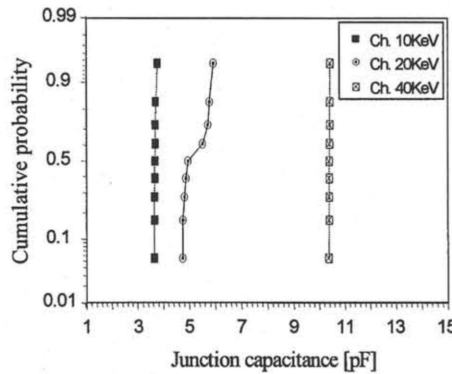

Fig. 3 N+/PW area junction capacitance with varying energy of boron n-channel

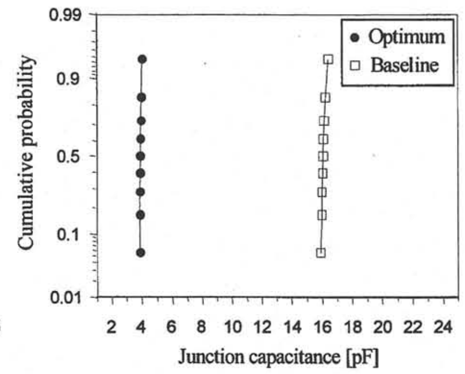

Fig. 4 P+/NW area junction capacitance for optimum vs. baseline condition

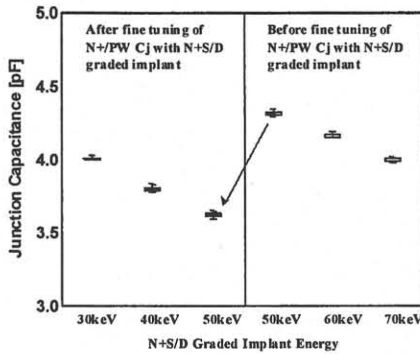

Fig. 5 N+/PW Cj reduction with respect to N+S/D graded implant condition

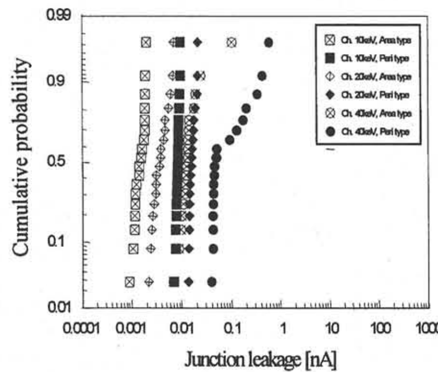

Fig. 6 N+/PW junction leakage current according to n-channel implantation

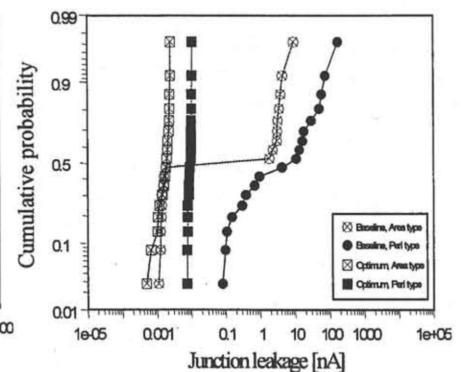

Fig. 7 P+/NW junction leakage current for optimum vs. baseline condition

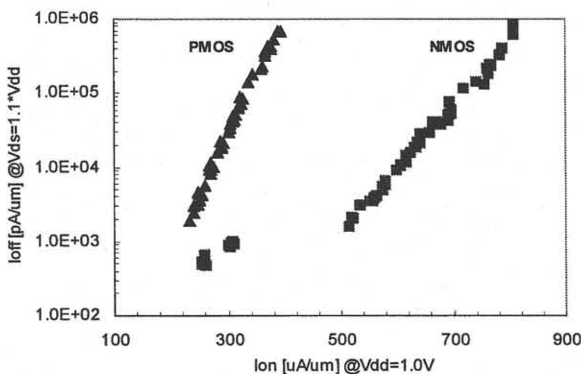

Fig. 8 Off-state current vs. drive current for NMOS and PMOS device with gate length 70nm at V_{DD}=1.0V

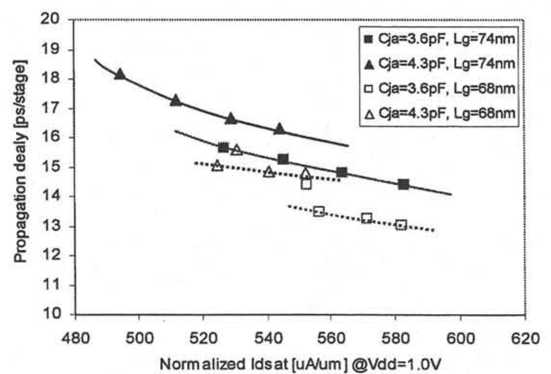

Fig. 9 Propagation delay vs. normalized Idsat with different junction capacitance and gate length