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Influence of Gate-to-Source Tunneling Current on Hot-Carrier Reliability Testing in MOSFETs with Ultra-Thin Gate Oxide

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1. Introduction

Hot-carrier reliability is a major reliability concern to continued device scaling. Accelerated testing of hot-carrier reliability is usually done under the worst-case stress condition. Recent studies show that either $V_g=V_d$ [1-2] or I_{submax} [3] is the worst-case stress condition. Thus, reliability testing is recommended to be performed at both $V_g=V_d$ and I_{submax}. As ultra-thin gate oxide is used in state-of-the-art CMOS technologies, one new concern arises when the device is stressed under $V_g=V_d$. Due to high electric field is applied between gate and source, the damage near the source side due to gate-to-source tunneling current may become comparable to the damage near the drain side caused by channel hot carriers [3-4]. To address this new concern, this paper investigates the significance of the damage caused by gate-to-source tunneling current during $V_g=V_d$ stress. Further, a model was established to estimate the impact of gate-to-source tunneling current on the results of $V_g=V_d$ stress.

2. Experiments

nMOSFETs and pMOSFETs with 0.15μm gate length and 2nm gate oxide thickness were fabricated with a 0.15μm CMOS process. Gate width of the devices is 10μm. The forward-mode saturation I_d measured at $V_g=V_d=V_{DD}=\pm1.2V$ was monitored. Devices were stressed at room temperature under various V_g with $V_d=V_g$ or $V_d=0V$. The stressing was interrupted periodically to measure I_d degradation. Lifetime is defined as the time to reach 5% degradation in I_d.

3. Results and Discussion

I_d degradation of nMOSFETs and pMOSFETs under $V_g=V_d$ stress and FN stress is shown in Fig. 1, and two distinct trends are observed. First, gate-to-source tunneling current has negligible impact on the results of $V_g=V_d$ stress for nMOSFETs, but not negligible for pMOSFETs. Assuming the amount of damage due to gate-to-source tunneling current during $V_g=V_d$ stress is half of the damage under pure FN stress. When the device reaches 5% I_d degradation during $V_g=V_d$ stress, the amount of I_d degradation caused by gate-to-source tunneling current is 0.006% and 0.6% for nMOSFETs and pMOSFETs, respectively. Such a phenomenon mainly results from lower stress $|V_g|$ in nMOSFETs (2.3V) than that of pMOSFETs (2.75V). Since the mean free path of electrons is about twice that of holes [5], electrons can gain high enough energy to create damage under a smaller $|V_d|$ ($=|V_g|$) during $V_g=V_d$ stress.

Second, FN-stress-induced I_d degradation of nMOSFETs is lower in smaller $|V_g|$ stress but is projected to be greater than that of pMOSFETs when $|V_g|>3.7V$. To explain this phenomenon, carrier-separation experiment [6] was performed under inversion conditions on nMOSFETs and pMOSFETs. The hole component (I_{gh}) and electron component (I_{ge}) of the tunneling gate current are drawn in Fig. 2. As seen in Fig. 1 and Fig. 2, the similarity of crossover in FN-stress-induced I_d degradation and I_{gh} around $|V_g|=3.7V$ suggests that I_d degradation due to FN stress is mainly caused by I_{gh}. Such an inference is not surprising because hole is two orders of magnitude more effective than electron in activating traps which cause oxide breakdown [7]. According to the analysis above, I_{gh} during stress is used to model pMOSFET's FN-stress-induced I_d degradation as follows:

$$-(\Delta I_d/I_d)_{FN} = (A_1)(I_{gh}^{m_1})(t^{n_1}) \quad (1)$$

A_1, m_1, n_1 are technology-dependent parameters, and t is stress time. In our samples, $A_1=2.0\times10^{18}$, $m_1=2.53$, and $n_1=0.30$ can model degradation data well as seen in Fig. 3.

To estimate the impact of gate-to-source tunneling current on the results of $V_g=V_d$ stress, modeling of I_d degradation under $V_g=V_d$ stress is also required. Since the total damage in the device is the sum of damage due to source-to-gate tunneling current and damage due to channel hot carriers, I_d degradation for pMOSFETs under $V_g=V_d$ stress is modeled as follows:

$$-(\Delta I_d/I_d)_{Vg=Vd} = 0.5\times(-\Delta I_d/I_d)_{FN} + (A_2)(I_g^{m_2})(t^{n_2}) \quad (2)$$

A_2, m_2, and n_2 are also technology-dependent parameters. Note that gate current (I_g) during stress is used to model I_d degradation resulted from channel hot carriers because device degradation under $V_g=V_d$ stress is mainly caused by hot-hole injection [8]. As seen in Fig. 4, model and data also matched pretty well when $A_2=1.8\times10^7$, $m_2=1.09$, and $n_2=0.32$ are used in (2).

According to measured I_{gh} vs. V_g and I_g vs. V_g relationship (shown in Fig. 5), lifetime as a function of V_g under $V_g=V_d$ stress can be solved as a self-consistent solution for (1) and (2). Once the lifetime is obtained, the amount of I_d degradation caused by gate-to-source tunneling current can be estimated as half of the value in (1). Results of the above modeling are shown in Fig. 6. Data of lifetime under $V_g=V_d$ stress and half of the I_d degradation under FN stress for the pMOSFETs in Fig. 1 are also included in Fig. 6 to show that the above modeling is reasonably accurate. Fig. 6 reveals that I_d degradation resulted from gate-to-source tunneling current during $V_g=V_d$ stress is reduced when the stress $|V_g|$ is lower. Specifically, if $V_g=V_d$ stress is done under $|V_g|<1.95V$, I_d degradation due to gate-to-source tunneling current is less than 0.25%, i.e. less than 5% of the total I_d degradation.

4. Conclusions

The impact of gate-to-source tunneling current on the results of $V_g=V_d$ stress is negligible for nMOSFETs, but not negligible for pMOSFETs. pMOSFET's I_d degradation caused by FN stress and $V_g=V_d$ stress can be modeled by the hole component of the tunneling gate current and hot-hole gate current. To reduce the impact of gate-to-source tunneling current on the results of $V_g=V_d$ stress, stressing should be done under a lower $|V_d|$ ($=|V_g|$).

Acknowledgment

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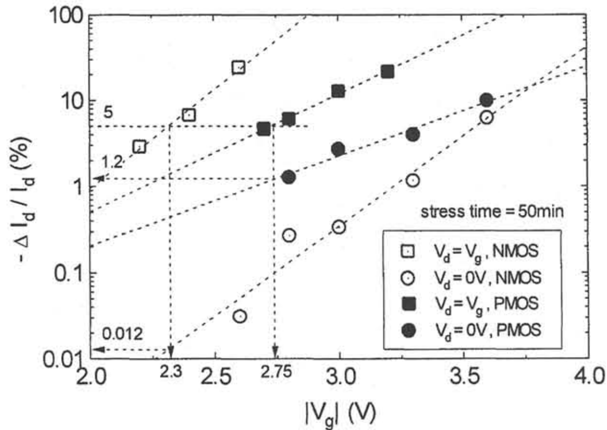

Fig.1 I_d degradation of nMOSFETs and pMOSFETs under V_g=V_d stress and FN stress. The impact of gate-to-source tunneling current on the results of V_g=V_d stress is negligible for nMOSFETs, but not negligible for pMOSFETs.

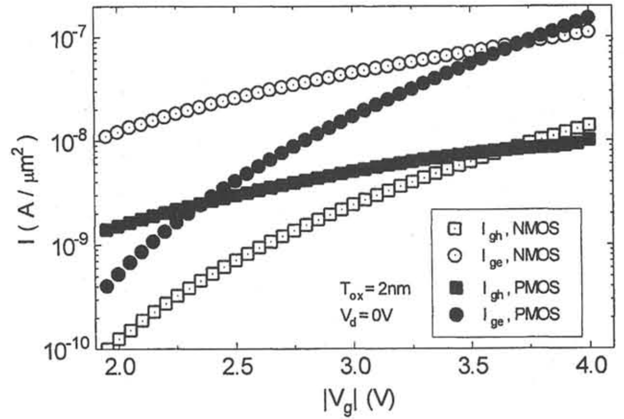

Fig. 2 Hole component (I_{gh}) and electron component (I_{ge}) of the tunneling gate current for nMOSFETs and pMOSFETs. Around $|V_g|$=3.7V, crossover of I_{gh} and FN-stress-induced I_d degradation (in Fig. 1) between nMOSFETs and pMOSFETs is observed.

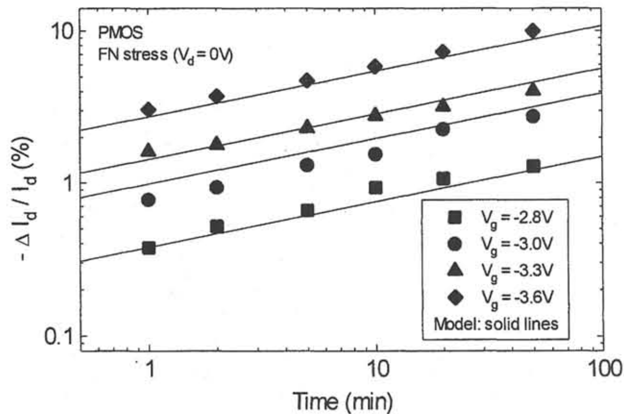

Fig. 3 Model and data of I_d degradation for pMOSFETs under FN stress at various stressing V_g. Good fitting is obtained.

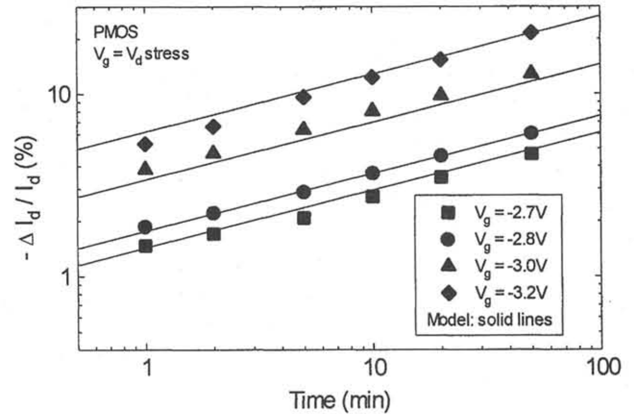

Fig. 4 Model and data of I_d degradation for pMOSFETs under V_g=V_d stress at various stressing V_g. The fitting is also well.

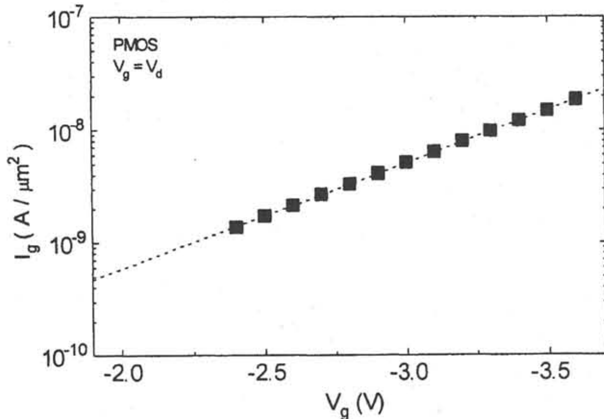

Fig. 5 The relationship between gate current and V_g under the condition of V_g=V_d for pMOSFETs.

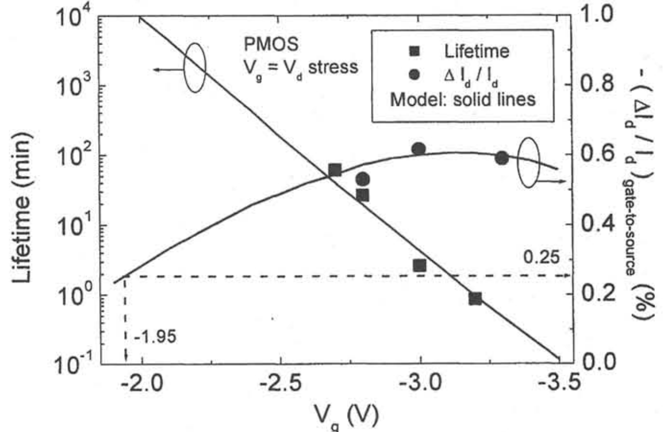

Fig. 6 Model and data of lifetime for pMOSFETs under V_g=V_d stress. When the device reaches its lifetime, the amount of I_d degradation caused by gate-to-source tunneling current is also estimated. This I_d degradation is reduced when the stress $|V_g|$ (=$|V_d|$) is lower.