Influence of Gate-to-Source Tunneling Current on Hot-Carrier Reliability Testing in MOSFETs with Ultra-Thin Gate Oxide

Jone F. Chen, Chih-Pin Tiao, and T.-C. Ong*
Department of Electrical Engineering and Institute of Microelectronics, National Cheng Kung University, Tainan, Taiwan 70101, Tel: 886-6-275-7575, E-mail: jfchen@mail.ncku.edu.tw
* Logic Technology Division, TSMC, Hsin-Chu, Taiwan

1. Introduction
Hot-carrier reliability is a major reliability concern to continued device scaling. Accelerated testing of hot-carrier reliability is usually done under the worst-case stress condition. Recent studies show that either \( V_{G}=V_{th} \) [1-2] or \( V_{G}=I_{thmax} \) [3] is the worst-case stress condition. Thus, reliability testing is recommended to be performed at both \( V_{G}=V_{th} \) and \( V_{G}=I_{thmax} \). As ultra-thin gate oxide is used in state-of-the-art CMOS technologies, one new concern arises when the device is stressed under \( V_{G}=V_{th} \). Due to high electric field is applied between gate and source, the damage near the source side due to gate-to-source tunneling current may become comparable to the damage near the drain side caused by channel hot carriers [3-4]. To address this new concern, this paper investigates the significance of the damage caused by gate-to-source tunneling current during \( V_{G}=V_{th} \) stress. Further, a model was established to estimate the impact of gate-to-source tunneling current on the results of \( V_{G}=V_{th} \) stress.

2. Experiments
nMOSFETs and pMOSFETs with 0.15μm gate length and 2nm gate oxide thickness were fabricated with a 0.15μm CMOS process. Gate width of the devices is 10μm. The forward-mode saturation \( I_{S} \) measured at \( V_{G}=V_{th} \) and \( V_{D}=V_{DD}=1.2V \) was monitored. Devices were stressed at room temperature under various \( V_{G} \) with \( V_{G}=V_{th} \) or \( V_{G}=0V \). The stressing was interrupted periodically to measure \( I_{S} \) degradation. Lifetime is defined as the time to reach 5% degradation in \( I_{S} \).

3. Results and Discussion
\( I_{S} \) degradation of nMOSFETs and pMOSFETs under \( V_{G}=V_{th} \) stress and FN stress is shown in Fig. 1, and two distinct trends are observed. First, gate-to-source tunneling current has negligible impact on the results of \( V_{G}=V_{th} \) stress for nMOSFETs, but not negligible for pMOSFETs. Assuming the amount of damage due to gate-to-source tunneling current during \( V_{G}=V_{th} \) stress is half of the damage under pure FN stress. When the device reaches 5% \( I_{S} \) degradation during \( V_{G}=V_{th} \) stress, the amount of \( I_{S} \) degradation caused by gate-to-source tunneling current is 0.006% and 0.6% for nMOSFETs and pMOSFETs, respectively. Such a phenomenon mainly results from lower stress \( |V_{d}| \) in nMOSFETs (2.3V) than that of pMOSFETs (2.75V). Since the mean free path of electrons is about twice that of holes [5], electrons can gain high enough energy to create damage under a smaller \( |V_{d}| \) during \( V_{G}=V_{th} \) stress.

Second, FN-stress-induced \( I_{S} \) degradation of nMOSFETs is lower in smaller \( |V_{d}| \) stress but is projected to be greater than that of pMOSFETs when \( |V_{d}| \geq 3.7V \). To explain this phenomenon, carrier-separation experiment [6] was performed under inversion conditions on nMOSFETs and pMOSFETs. The hole component (\( I_{ph} \)) and electron component (\( I_{pe} \)) of the tunneling gate current are drawn in Fig. 2. As seen in Fig. 1 and Fig. 2, the similarity of crossover in FN-stress-induced \( I_{S} \) degradation and \( I_{ph} \) around \( |V_{d}|=3.7V \) suggests that \( I_{ph} \) degradation due to FN stress is mainly caused by \( I_{ph} \). Such an inference is not surprising because hole is two orders of magnitude more effective than electron in activating traps which cause oxide breakdown [7]. According to the analysis above, \( I_{ph} \) during stress is used to model pMOSFET's FN-stress-induced \( I_{S} \) degradation as follows:

\[
-\left(\frac{\Delta I_{S}}{I_{S}}\right)_{V_{G}=V_{th}} = \frac{A_{1}I_{ph}(t)\left(t^{*}\right)}{A_{2}}, \quad m_{1}, n_{1}
\]

where \( m_{1}, n_{1} \) are technology-dependent parameters, and \( t \) is stress time. In our case, \( A_{1}=2.0\times10^{-18} \), \( m_{1}=2.53 \), and \( n_{1}=0.30 \) can model degradation data well as seen in Fig. 3.

To estimate the impact of gate-to-source tunneling current on the results of \( V_{G}=V_{th} \) stress, modeling of \( I_{S} \) degradation under \( V_{G}=V_{th} \) stress is also required. Since the total damage in the device is the sum of damage due to source-to-gate tunneling current and damage due to channel hot carriers, \( I_{S} \) degradation for pMOSFETs under \( V_{G}=V_{th} \) stress is modeled as follows:

\[
-\left(\frac{\Delta I_{S}}{I_{S}}\right)_{V_{G}=V_{th}} = \frac{0.5\times(-\Delta I_{S}/I_{S})_{V_{G}=V_{th}} + (A_{2})(I_{ph}(t)\left(t^{*}\right))}{A_{2}}, \quad m_{2}, n_{2}
\]

where \( m_{2}, n_{2} \) are technology-dependent parameters. Note that gate current \( I_{G} \) during stress is used to model \( I_{S} \) degradation resulted from channel hot carriers because device degradation under \( V_{G}=V_{th} \) stress is mainly caused by hot-hole injection [8]. As seen in Fig. 4, model and data also matched pretty well when \( A_{2}=1.8\times10^{-17} \), \( m_{2}=1.09 \), and \( n_{2}=0.32 \) are used in (2).

According to measured \( I_{ph} \) vs. \( V_{G} \) and \( I_{S} \) vs. \( V_{G} \) relationship (shown in Fig. 5), lifetime as a function of \( V_{G} \) under \( V_{G}=V_{th} \) stress can be solved as a self-consistent solution for (1) and (2). Once the lifetime is obtained, the amount of \( I_{S} \) degradation caused by gate-to-source tunneling current can be estimated as half of the value in (1). Results of the above modeling are shown in Fig. 6. Data of lifetime under \( V_{G} \) stress and half of the \( I_{S} \) degradation under FN stress for the pMOSFETs in Fig. 1 are also included in Fig. 6 to show that the above modeling is reasonably accurate. Fig. 6 reveals that \( I_{S} \) degradation resulted from gate-to-source tunneling current during \( V_{G}=V_{th} \) stress is reduced when the stress \( |V_{d}| \) is lower. Specifically, if \( V_{G}=V_{th} \) stress is done under \( |V_{d}|<1.95V \), \( I_{S} \) degradation due to gate-to-source tunneling current is less than 0.25%, i.e. less than 5% of the total \( I_{S} \) degradation.

4. Conclusions
The impact of gate-to-source tunneling current on the results of \( V_{G}=V_{th} \) stress is negligible for nMOSFETs, but not negligible for pMOSFETs. pMOSFET's \( I_{S} \) degradation caused by FN stress and \( V_{G}=V_{th} \) stress can be modeled by the hole component of the tunneling gate current and hot-hole gate current. To reduce the impact of gate-to-source tunneling current on the results of \( V_{G}=V_{th} \) stress, stressing should be done under a lower \( |V_{d}| \).

Acknowledgment
This work was supported in part by NSC under contract NSC90-2215-E-006-019.
Fig. 1  $I_d$ degradation of nMOSFETs and pMOSFETs under $V_g=V_d$ stress and FN stress. The impact of gate-to-source tunneling current on the results of $V_g=V_d$ stress is negligible for nMOSFETs, but not negligible for pMOSFETs.

Fig. 2 Hole component ($I_{dh}$) and electron component ($I_{de}$) of the tunneling gate current for nMOSFETs and pMOSFETs. Around $|V_g|=3.7$V, crossover of $I_{dh}$ and FN-stress-induced $I_d$ degradation in Fig. 1 between nMOSFETs and pMOSFETs is observed.

Fig. 3 Model and data of $I_d$ degradation for pMOSFETs under FN stress at various stressing $V_g$. Good fitting is obtained.

Fig. 4 Model and data of $I_d$ degradation for pMOSFETs under $V_g=V_d$ stress at various stressing $V_g$. The fitting is also well.

Fig. 5 The relationship between gate current and $V_g$ under the condition of $V_g=V_d$ for pMOSFETs.

Fig. 6 Model and data of lifetime for pMOSFETs under $V_g=V_d$ stress. When the device reaches its lifetime, the amount of $I_d$ degradation caused by gate-to-source tunneling current is also estimated. This $I_d$ degradation is reduced when the stress $|V_g|$ (=|$V_d$|) is lower.