Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 392-393

P2-5

Nano-Roughness Enhanced Reliability of MOS Tunneling Diodes

F. Yuan, C.-H. Lin, C.-R. Shie, K.-F. Chen, M. H. Lee, and C. W. Liu[a]
Graduate Institute of Electronics Engineering and Department of Electrical Engineering,
National Taiwan University, Taipei, Taiwan
[a](Tel) 886-2-23635251 ext. 515 (Fax) 886-2-23638247 (E-mail) chee@cc.ee.ntu.edu.tw

1. Introduction

The improvement of lithography has enabled smaller geometry devices and a higher level of circuit integration. When the devices scale down to deep-submicron, oxide reliability becomes a major concerned issue. Nakanishi et al. have proposed the surface roughness of interface degraded the time-dependent dielectric breakdown (TDDB) characteristics of MOS capacitors with F-N tunneling current through the oxide, and enhance the tunneling current through the oxide [1]. The interface roughness also degraded MOSFET channel mobility due to the surface scattering [2,3]. However, it is reported that the nano-roughness enhanced electro-luminescence efficiency in the MOS tunneling diodes [4]. In this paper, we investigate the oxide nano-roughness effect on oxide reliability in MOS tunneling diodes. Both electrical and optical reliabilities of MOS tunneling diodes are enhanced by oxide nano-roughness.

2. Experiments

The 4-inch Si wafer was cleaned by a HF dip, and the rough oxide was achieved by very high vacuum prebake ($<3x10^{-6}$ torr, maintained by a turbo pump) before the growth of ultrathin gate oxide. The wafer was baked in H_2 (or D_2) to incorporate hydrogen (or deuterium) before and after the rapid thermal oxidation (RTO). The MOS tunneling diodes have aluminum gate electrodes with circular areas defined by photolithography. The interface roughness and surface roughness were measured by atomic force microscopy (AFM). The oxide thickness was measured by ellipsometry. The current-voltage (I-V) and constant voltage stress (CVS) measurements were carried out by using an HP-4156A semiconductor parameter analyzer.

3. Results and Discussion

The AFM measurement shows the oxide surface morphology on the Si wafer without (Fig. 1(a)) and with (Fig. 1(b)) very high vacuum prebake process. The root mean square (rms) value of oxide nano-roughness is 0.06 nm and 0.85 nm, respectively. The roughness magnitude of oxide surface is very similar to that of the oxide/silicon interface. This confirms the conformal growth of the oxide [5]. Fig. 2 shows the time evolutions of the gate tunneling current for the flat and the rough NMOS tunneling diodes with the same oxide thickness of 1.6 nm, under CVS at gate voltage (V_g) of -3V. The flat NMOS device reveals soft breakdown after ~1800 sec stress, while the rough NMOS devices shows very little gate current fluctuation under the same stress condition. The Weibull plots of Q_{BD} and T_{BD} characteristics for both the flat (H_2) and the rough (H_2) NMOS tunneling diodes under CVS at V_g=-3V are shown in Fig. 3&4, which indicates the enhanced reliability by the nano-roughness. There are 2.9 and 4.9 fold enhancement in Q_{BD} and T_{BD}, respectively, at 63% failure rate. The deuterium isotope effect has been investigated by many groups for years, but no isotope effect has been observed in the D_2-treated MOS devices stressed in the hole injection condition [6]. As mentioned in Fig. 6&7, the deuterium doesn't improve the oxide reliability of PMOS tunneling diodes under the hole injection stress. The tunneling-hole-induced traps in bulk oxide are responsible for this soft breakdown (Fig. 8), and oxide degrades even with the deuterium passivation [6]. Therefore, it is of great importance and interest to improve the reliability of ultrathin gate oxide in PMOS tunneling diodes. The Weibull plots of Q_{BD} and T_{BD} characteristics for PMOS tunneling diodes indicate the enhanced reliability by the nano-roughness. There are 5.7 and 2.5 fold enhancement in Q_{BD} and T_{BD}, respectively, at 63% failure rate (Fig. 6&7). The nano-roughness may be an alternative to improve the PMOS tunneling diodes reliability.

The speculative mechanism of enhanced oxide reliability with oxide nano-roughness is shown in Fig. 9. When the carriers tunnel through the oxide, they are scattered by the oxide nano-roughness and the energy perpendicular to the interface of the injected carriers is reduced. Since the reliability of the MOS tunneling diode is related to the energy of the injected carriers, the energy reduction of the carriers tunneling through the oxide improves the electrical reliability of the devices.

To further investigate the effect of oxide nano-roughness on reliability, the light emission at bandgap energy [7] is measured. The diode area is $5x10^{-3}$ cm^2 and the driving current is -100mA. The emission intensity of the H_2-treated flat NMOS tunneling diode degrades 20% after 1400 sec stress. However, the rough device reveals a very slight variation during the stress time (Fig. 10). The PMOS tunneling diodes show the similar result (Fig. 11). The degradation of light emission indicates the formation of interface states, which act as non-radiative recombination centers to degrade the emission intensity. This indicates that more interface states are generated in the flat MOS device than in the rough MOS device. Fig.12 shows that the MOS LED quantum efficiency increases when the oxide nano-roughness increases. Due to the indirect bandgap nature of Si, additional momentum is required for the light emission process, which can be provided by the phonon scattering and oxide roughness scattering [4]. The emission efficiency can be enhanced by the oxide nano-roughness.

4. Conclusions

The ultrathin oxide reliability can be enhanced by introducing oxide nano-roughness. The oxide nano-roughness reduces the impact electron/hole energy perpendicular to the Si/SiO_2 interface, and decreases voltage acceleration factor. The rough oxide can be a novel technology to improve both the electrical and optical reliability of MOS devices.

Acknowledgments

This work is supported by NSC, Taiwan, R.O.C.
(NSC 90-2212-E-002-226, NSC 90-2215-E-002-034)

References

[1] T. Nakanishi et al., Tech. Dig., VLSI 1989, pp. 79-82.
[2] T. Yamanaka et al., IEEE EDL 1996, pp. 178-180.
[3] J. Koga et al., Tech. Dig., IEDM 1994, pp.475-478.
[4] C. W. Liu et al., IEEE EDL 2000, pp. 601-603.
[5] V. Tsai et al., Appl. Phys. Lett., **71** (11), pp. 1495-1497, 1997.
[6] K. Deguchi et al., Tech. Dig., IEDM 2000, pp. 327-330.
[7] C. W. Liu et al., Tech. Dig., IEDM 1999, pp.749-752.

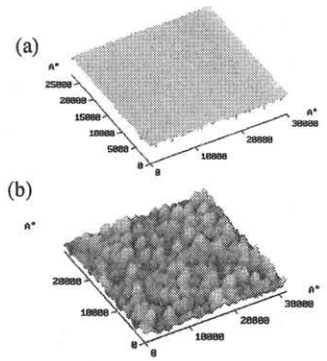

Fig. 1. (a) The AFM image of oxide without very high vacuum prebake. (rms value of nano-roughness=0.06 nm) (b) The AFM image of oxide with very high vacuum prebake. (rms value of nano-roughness=0.85 nm).

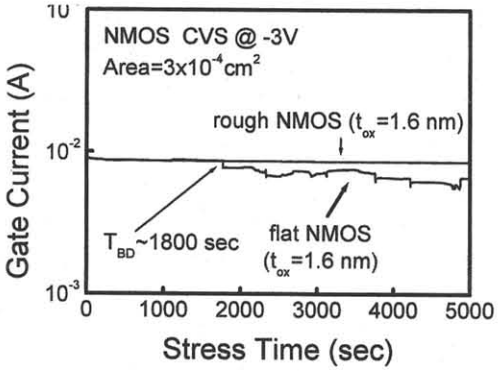

Fig. 2. The time evolutions of gate current of the flat and the rough NMOS tunneling diodes under -3V constant voltage stress. The flat NMOS device reveals soft breakdown after ~1800 sec stress.

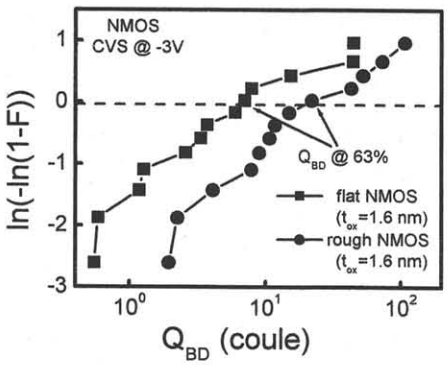

Fig. 3. The Weibull plot of the charge to breakdown (Q_{BD}) characteristics for the flat (H_2) (rms value of nano-roughness=0.06nm) and the rough (H_2) (rms value of nano-roughness=0.85nm) NMOS tunneling diodes under CVS at V_g=-3V.

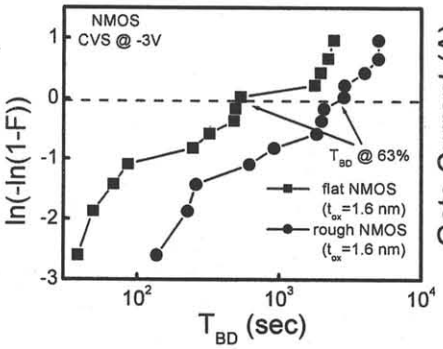

Fig. 4. The Weibull plot of the time to breakdown (T_{BD}) characteristics for the flat (H_2) and the rough (H_2) NMOS tunneling diodes under CVS at V_g=-3V.

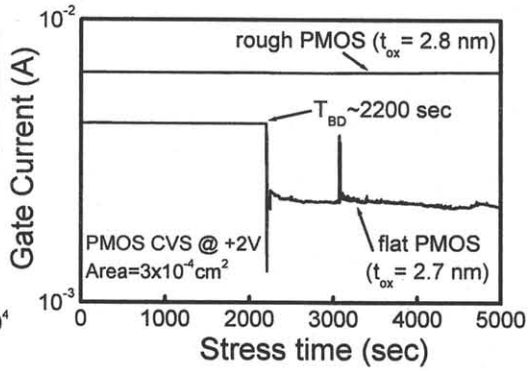

Fig. 5. The time evolutions of gate current of the flat and the rough PMOS tunneling diodes under 2V constant voltage stress. The flat PMOS device reveals soft breakdown after ~2200 sec stress.

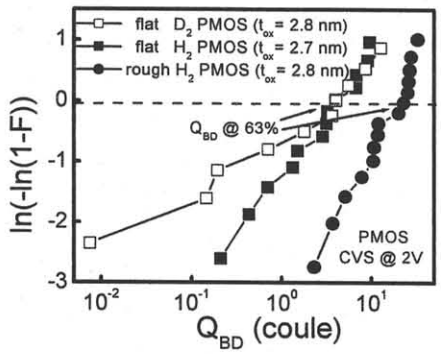

Fig. 6. The Weibull plot of the Q_{BD} characteristics for the flat (H_2, D_2) (rms value of nano-roughness=0.15nm) and the rough (H_2) (rms value of nano-roughness=1.46nm) PMOS tunneling diodes under CVS at V_g=2V.

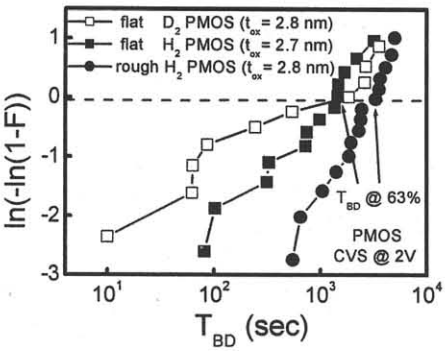

Fig. 7. The Weibull plot of the T_{BD} characteristics for the flat (H_2, D_2) and the rough (H_2) PMOS tunneling diodes under CVS at V_g=2V.

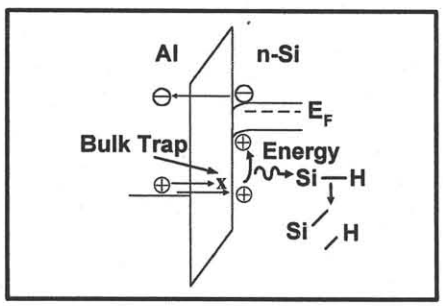

Fig. 8. Two mechanisms of soft breakdown in the PMOS tunneling diode. The hole tunneling from the Al to Si may break Si-H bond at interface and may be trapped in the bulk oxide by oxygen vacancy.

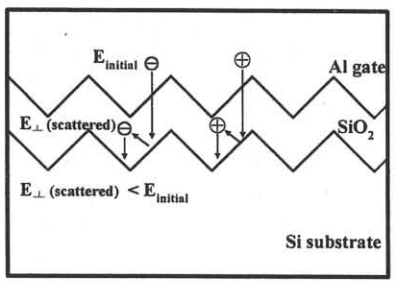

Fig. 9. The illustration of the speculative mechanism of the nano-roughness enhanced reliability. The impact energy perpendicular to the Si/SiO_2 of electron or hole is reduced due to the surface and interface roughness scattering.

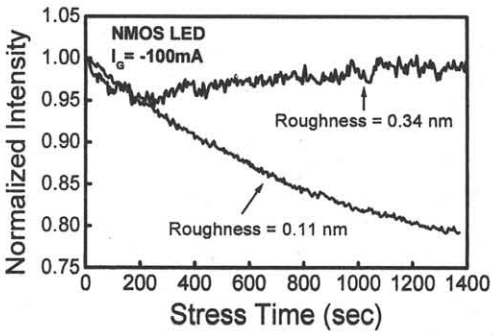

Fig. 10. The time evolutions of light emission intensity for the rough and flat NMOS LED. The intensity degrades about 20% after 1400 sec stress in the flat NMOS diode. However, the rough device reveals a very slight variation during the stress time.

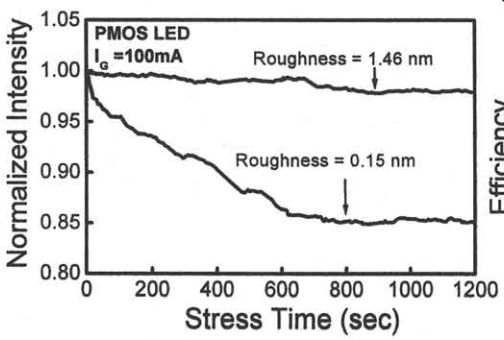

Fig. 11. The time evolutions of light emission intensity for the rough and flat PMOS LED. The intensity degrades about 15% after 1200 sec stress in the flat PMOS diode The rough PMOS diode shows much less emission intensity degradation as compared to the flat PMOS diode.

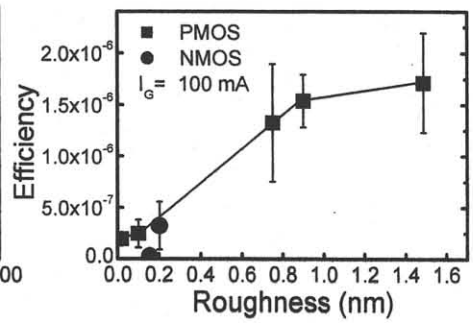

Fig. 12. The external quantum efficiency vs oxide roughness of MOS LED. The error bar is the standard deviation of external quantum efficiency measured by a set of devices. The devices with rougher oxide have larger light emission efficiency.