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An Optimization of the Anti-punchthrough Implant for ESD Protection Circuit Design

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1. Introduction

In recent years, anti-punchthrough (anti-P) has been used in suppressing the short channel effect [1,2]; however there is only few works concern about the improving electrostatic discharge (ESD) [3,4] robustness by using optimizing the implant. Therefore, choose and analyze a semiconductor device for the design of both efficient ESD protection circuit and internal circuit are important issues.

In this work, we applied a robust TCAD simulator [5] in the optimization of the anti-P implant of device for ESD circuit design. With this approach, a better ESD robustness could be achieved, and it could provide device engineer a useful platform to meet the requirements of device characteristics and ESD strength. To reduce the input capacitance, a VLSI circuit is also proposed and verified to eliminate the drawbacks of high parasitic capacitance caused from anti-P implant which is especially important in RF circuit design.

2. Experiments and Simulations

For studying ESD robustness of protection devices, we simulate 4 device types to calculate and determine the most attractive structure in ESD protection circuit. These device structures are shown in Figs. 1a-1d. The major difference among them is the location of the anti-P implantation. Fig. 1a is the device without anti-P implantation. Fig. 1b is with the anti-P implantation under the source/drain (S/D) extension. Fig. 1c shows the anti-P implantation under the deep S/D, and the device in Fig. 1d has an anti-P implantation over the junction area. The implantation of anti-P is boron with a concentration of 3e+17 (atoms/cm^{-3}). A set of device equations including the Poisson, carrier current continuity, carrier energy balance, and lattice equations are solved numerically [5]. With the developed simulator, we simulate the proposed devices to evaluate the characteristics for ESD design. Comparison among devices is reported; as a result, a suitable device could be characterized and advised.

3. Results and Discussion

To estimate ESD strength of the designed devices, the electron temperature (T_n) distributions are calculated and shown in Fig 2. In this figure, we can find that the device (d) has the lowest temperature among the devices; on the other hand, according to the Tab. 1, it has the highest current density under high voltage applied. That is, the device (d) can handle the largest current without resulting large heat generation. Thus it is the most suitable structure in ESD protection. Besides the value of maximum temperature in devices, the location of the local high temperature is also a critical item in determine the ESD robustness. In this point of view, the device has a better ESD robustness while the heat located far away from the interface surface. The maximum temperature and location of the heat are summarized in Tab. 2. We find that the device (d) is the best candidate. Tab. 3 shows the calculated parasitic capacitance. We see the device (a) has a slightly smaller parasitic capacitance. Even has a lower parasitic capacitance, the device (a) still cannot meet the requirement of microwave circuit and applications. The parasitic capacitance must be smaller than 0.2 fF/um [4]; unfortunately, all the MOSFET structures cannot meet this requirement. To reduce the parasitic capacitance, the circuit level design is included and shown in Fig. 3. With this circuit, we conclude the device (d) can obtain both high ESD robustness and low capacitance. We also observed Types 2 and 4 have lower DIBL effect and are less sensitive for hot carrier effects. Our simulation methodology provides an alternative for device structure optimization and applications in ESD protection circuitry performance improvements simultaneously.

4. Conclusions

We have introduced a simulation-based method to study device structures for improving ESD robustness and suppressing short channel effects simultaneously. It could minimize the design complexity, increase ESD performance and reduce chip size. The proposed simulation approach has high efficiency in device characterization and is especially useful for SOC design and circuit parameters extraction.

Acknowledgments

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References

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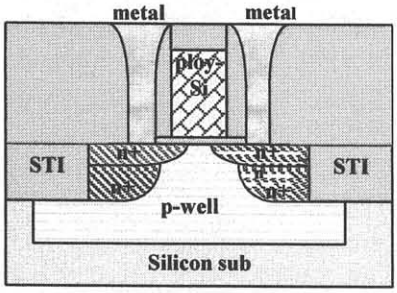

Fig. 1. (a) The proposed device structure Type 1 for the study.

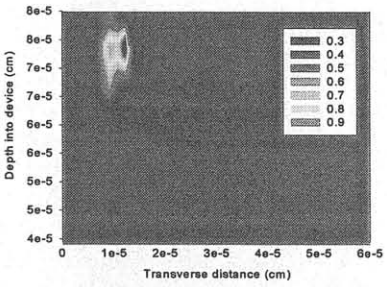

Fig. 2. (a) The simulated temperature profiles with respect to the Type 1 device structure.

Table 1. The computed I-V data and the corresponding maximum electron temperature distribution for the proposed Type 1 ~ 4 device structures @ V_{DS} = 7.0 V.

	Type 1	Type 2	Type 3	Type 4
Current density (mA/um)	0.82	0.91	1.25	1.57
Max T_n	11429 K	10310 K	9324 K	7879 K

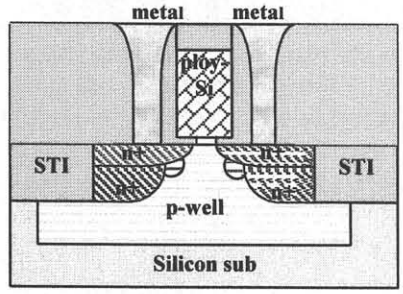

Fig. 1. (b) The proposed device structure Type 2 for the study.

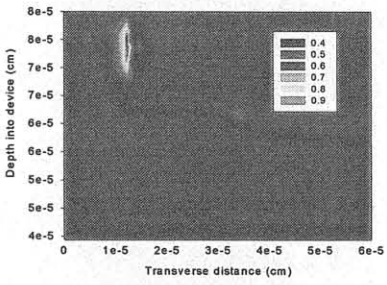

Fig. 2. (b) The simulated temperature profiles with respect to the Type 2 device structure.

Table 2. Corresponding to Table 1, the computed maximum electron temperature location is summarized. It is away from the channel surface.

	Type 1	Type 2	Type 3	Type 4
T_n location away from surface	13.0 nm	31.0 nm	61.3 nm	66.0 nm

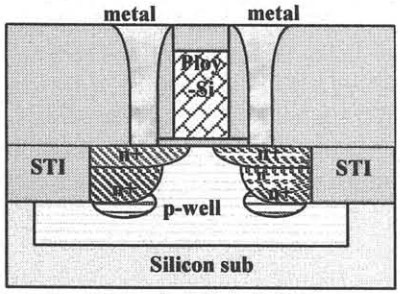

Fig. 1. (c) The proposed device structure Type 3 for the study.

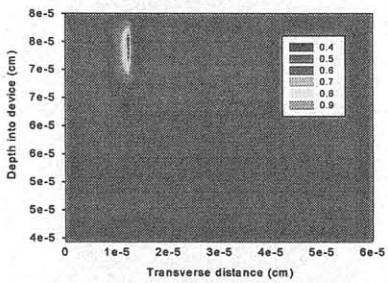

Fig. 2. (c) The simulated temperature profiles with respect to the Type 3 device structure.

Table 3. The computed capacitance $C = C_{DG} // C_{DB}$ for the 4 tested structures @ V_{DS} = 1.0 V. The C_{DG} is the capacitance between drain and gate; the C_{DB} is the capacitance of drain and substrate.

	Type 1	Type 2	Type 3	Type 4
Capacitance (fF/um)	6.0	6.3	6.6	8.7

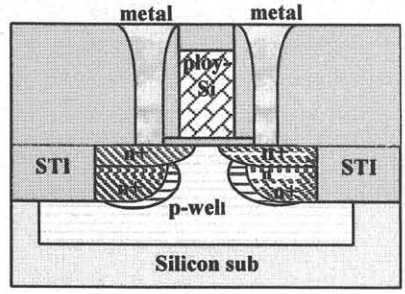

Fig. 1. (d) The proposed device structure Type 4 for the study.

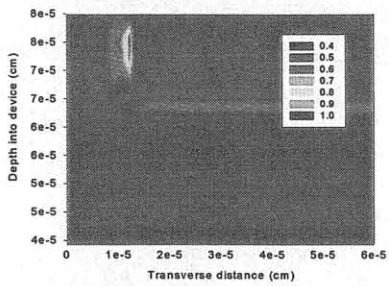

Fig. 2. (d) The simulated temperature profiles with respect to the Type 4 device structure.

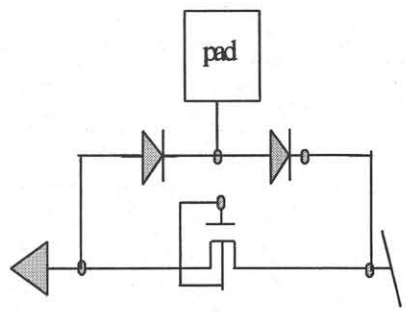

Fig. 3. The proposed ESD protection circuit.