Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, 2002, pp. 396-397

P2-7

Second Breakdown of 18V GGNMOS induced by Kirk Effect Under ESD

Byung-Chul Jeon, Seung-Chul Lee, Min-Koo Han
#50, 301-1115, School of Electrical Eng., Seoul Nat'l Univ., Shinlim-dong, Kwanak-ku, Seoul 151-742, Korea
Phone: +82-2-880-7254, Fax: +82-2-875-7254, e-mail: mkh@snu.ac.kr

1. Introduction

18V GGNMOS (Grounded-Gate NMOS) is widely employed as high-voltage output driver for color STN (Super Twisted Nematic) LDI (Liquid crystal display Driver IC). However, the ESD immunity properties of high-voltage GGNMOS have been scarcely reported although high-voltage output drivers such as LDMOS (Lateral Double diffused MOS) and DENMOS (Drain-Extended MOS) are highly vulnerable to ESD stress. The purpose of our work is to report the effects of design parameters on the ESD immunity characteristics of 18V GGNMOS fabricated via 0.35 μm design rule.

2. Experimental, Simulation Results and Discussion

Top and cross-sectional view of 18V high-voltage GGNMOS are shown in Fig. 1. A transmission line pulser (TLP) test system, Barth Model 4002^{TM} (Barth Electronics, Inc.) is employed to evaluate ESD behavior. Fig. 2 shows the experimental TLP I-V characteristics of conventional 18V GGNMOS and modified GGNMOS. Any snap-back behavior is not observed in the conventional one while snap-back is measured in the modified one. 2-D simulations employing ISE have been performed in order to investigate effects of design parameters on the ESD immunity level difference between the conventional and modified one. Design parameters of simulated GGNMOS are shown in Table. I.

Fig. 3 shows drain voltage (V_D) and maximum temperature (T_{MAX}) as function of time and I-V characteristics of J1, of which design parameters are identical to the conventional one and J5, of which design parameters are identical to the modified one. It is shown that I-V characteristics of both J1 and J5 not only exhibit the snap-back but is also similar to the well-known I-V characteristics of low-voltage GGNMOS although the current level of J5 at point K' ($I_{K'}$), which may be the second breakdown point of J5, is about two times higher than that of J1 at point K (I_K). However, maximum temperatures of J1 and J5 at point K and K' are 343K and 392K respectively, which is significantly less than second breakdown temperature of low-voltage GGNMOS.

In order to analyze unusual low-temperature second breakdown characteristics of 18V GGNMOS, three points in I-V curves are selected respectively on the same current density of J1 and J5, which are entitled as A, B and C. 2-dimensional distributions of total current density (J_D), maximum temperature (T_{MAX}), impact ionization rates (II) and electric field (EF) of J1 and J5 are compared at each point and shown in Fig. 6. It is observed that as current increases from A to C, the current density flowing through the left side of the n+ junction becomes higher and the locations of T_{MAX}, II and EF are moved to the left side of the n+ junction (at point C). These phenomena may be clearly explained by the well-known Kirk effect [1]. As the current density is increased, the increasing amount of charge related to the mobile carriers alters the space charge distribution and shifts the location where the peak electric field and maximum impact ionization rates occurs, to the left side of the n+ junction, which leads to current concentration near the region. As the current density is increased further, the peak electric field and maximum impact ionization rates become even higher and the current flow becomes considerably concentrated in the region, which results in hot spot as shown in Fig. 6. It should be noted that the increase of avalanche generation due to Kirk effect leads to the decrease of the drain voltage as shown in Fig. 3 under low temperature such as 340K.

Effects of XO on the I_K are analyzed by comparing the simulation results of J2, J3 and J4. Fig. 4 shows the V_D and T_{MAX} as function of time and I-V characteritics of J2, J3 and J4. It should be noted that drain voltage of J2 continuously diminishes after snap-back just like the measured data of the conventional GGNMOS, which can support that ESD failure mechanism of 18V GGNMOS is second breakdown induced by Kirk effect. The current level I_K, where Kirk effect induced second breakdown occurs, is increased with increading XO. It would be inferred that N-drift resistance between the channel edge and the n+ junction behaves as ballast resistance, which can subsequently divert current to the bottom of N-drift as shown in Fig. 7.

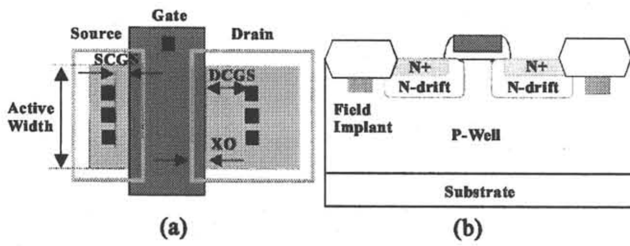
J4, J5 and J6 are compared in order to investigate effects of DCGS on the I_K of 18V GGNMOS. Fig. 5 shows V_D and T_{MAX} as function of time and I-V characteritics of J4, J5 and J6. 2D-simulation results that I_K of J6 is about two times higher than that of J4. When DCGS is increased, the n+ resistance from the left side of the n+ junction to the drain contact is also increased linearly, which can divert more current to the bottom of n+ junction as shown in Fig. 8.

3. Conclusion

Effects of design parameters on the ESD immunity characteristics of 18V GGNMOS fabricated via 0.35 μm technology are investigated employing TLP test and simulation. Experimental and simulation results show that the ESD failure mechanism in 18V GGNMOS is the low-temperature second breakdown induced by Kirk effect. We have successfully obtained high ESD immunity current level (I_K) of 18V GGNMOS by optimizing design parameters. The ballast resistance, which is increased with increasing XO and DCGS, is crucial for diverting current flow to the bottom of n+ junction, which alleviates Kirk effect.

References

[1] A. Ludikhuize et al, ISPSD, pp.153-156, 2000.



(a) (b)

Figure 1: (a) Top and (b) cross sectional view of 18V GGNMOS

Table I: The layout design parameter of splitted GGNMOS

	XO	DCGS	SCGS	Lgate
J1	0.2 μm	0.85 μm	0.85 μm	3.0 μm
J2	0.0 μm	0.85 μm	1.0 μm	4.0 μm
J3	0.2 μm	0.85 μm	1.0 μm	4.0 μm
J4	0.5 μm	0.85 μm	1.0 μm	4.0 μm
J5	0.5 μm	1.5 μm	1.0 μm	4.0 μm
J6	0.5 μm	3.0 μm	1.0 μm	4.0 μm

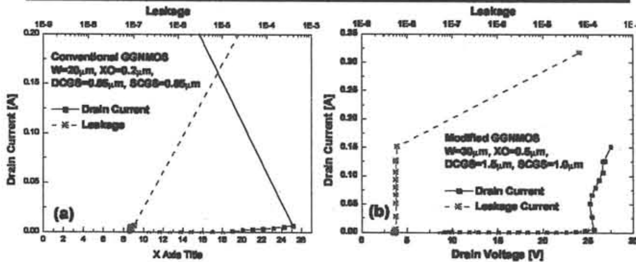


Figure 2: TLP I-V characteristics of (a) conventional GGNMOS and (b) modified GGNMOS.

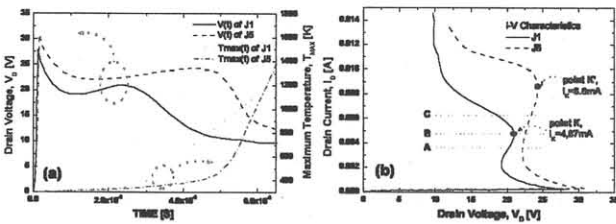


Figure 3: (a) drain voltage and maximum temperature as function of time and (b) I-V characteristics of J1 and J5.

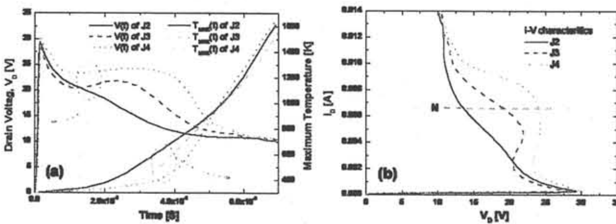


Figure 4: (a) drain voltage and maximum temperature as function of time and (b) I-V characteristics of J2, J3 and J4.

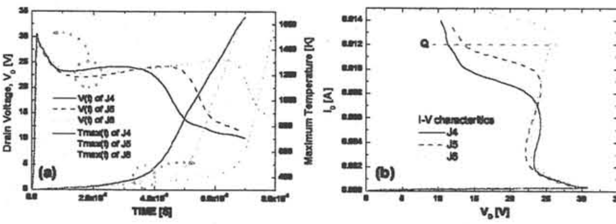
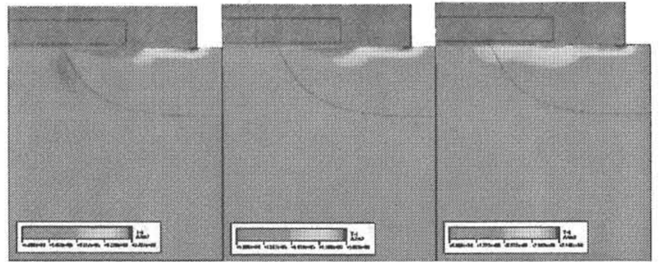
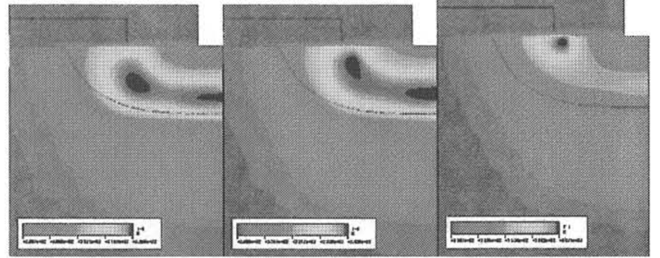


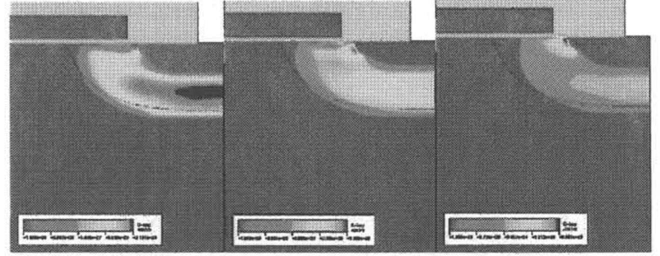
Figure 5: (a) drain voltage and maximum temperature as function of time and (b) I-V characteristics of J4, J5 and J6.



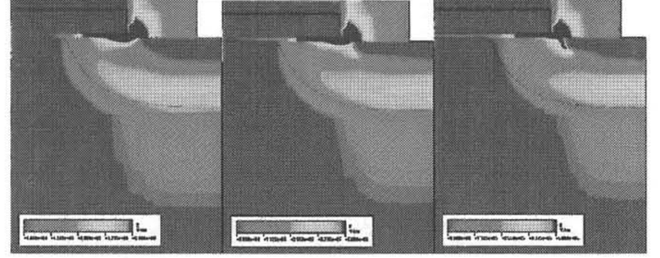
(i) J_D at point A point B point C



(ii) T_{MAX} at point A point B point C

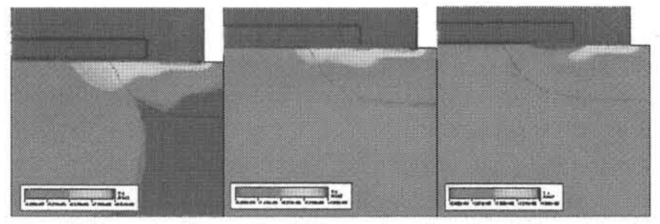


(iii) II at point A point B point C



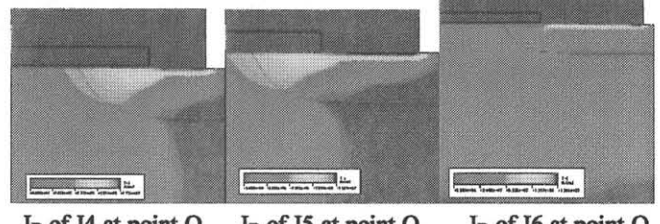
(iv) EF at point A point B point C

Figure 6: Distributions of J_D, T_{MAX}, II and EF of J1 from A to C



J_D of J2 at point N J_D of J3 at point N J_D of J4 at point N

Figure 7: 2-D distributions of J_D of J2, J3 and J4 at point N.



J_D of J4 at point Q J_D of J5 at point Q J_D of J6 at point Q

Figure 8: 2-D distributions of J_D of J4, J5 and J6 at point Q.