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P2-8

A New Trenched Source power MOSFET Improving Avalanche Energy

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1. Introduction

Power MOSFETs are widely used in various high voltage and high current applications. It is well known that low conduction and switching losses are essential in power MOSFET. They are also required to exhibit an avalanche capability that would prevent the parasitic bipolar transistor from activating under a high voltage and current condition.

The failure of the MOSFETs during the unclamped inductive switching (UIS) is due to the turn-on of the parasitic bipolar transistor under the high voltage and the high current condition [1]. Several methods have been already reported to prevent the activation of the parasitic bipolar transistor. One is to reduce the resistance of the p-body beneath the n+ source using high-energy implantation and/or employing sidewall process. However, it is rather difficult to control the doping concentration and the geometry of sidewall without altering the threshold voltage [2]. Another is to divert the direction of the current flow from the edge to the bottom of the p-body employing the split well structure or adding p+ distributed diodes which resulting in an additional device area for the p+ well [1][3].

In this paper, we proposed a new power MOSFET employing a deep body contact (DBC). Our simulation results show that the avalanche capability of the proposed device is improved considerably compared with that of the conventional one without increasing device area.

2. Device Structures

The cross-sectional view of the conventional (using distributed diode) and the proposed device is shown in Fig. 1. We have optimized the depth and width of the DBC to satisfy the rated voltage so that the avalanche energy is improved and the device area is minimized. The optimum device parameters are listed in Table I.

3. Unclamped Inductive Switching

The UIS test as shown in Fig. 2 is widely used to investigate the ruggedness of the power devices. The drain voltage and current of the power MOSFET in the measured and simulation during the UIS are shown in Fig. 3.

It should be noted that the impact ionization determines the current path during the UIS. After the gate voltage is removed, the breakdown of the conventional device occurs at the curved region of the p-body due to the electric field crowding so that the current flows through the p-body beneath the n+ source [4]. The total discharge time of the measured device (conventional) is slightly less than the simulation results due to the loss of external circuit [5]. On the contrary, that of the proposed device is induced under the bottom of the p-body due to the DBC as shown in Fig. 4. The current density beneath the n+ source is compared in Fig. 5. The current density of the conventional device exhibits 5 times higher than that of the proposed device. The small current density of the proposed device suppresses the possibility of the turn on the parasitic bipolar transistor remarkably.

4. Optimization of the Deep Body Contact

Although the DBC decreases the breakdown voltage slightly, the direction of the current flow under the UIS is diverted. 2D simulations by MEDICI as a function of the depth and width of the DBC were performed in order to have the optimum design. Fig. 6 shows that the optimum depth and width are found to be 1.2μm and 0.75μm, respectively. When the depth is less than 1.1μm, the depletion layer does not extend to the DBC in the breakdown regime. In this case, the breakdown occurs at the same position in the edge of the p-body. Therefore, the DBC has to be larger than the critical depth to improve the UIS characteristics. When the depth is deeper than 1.1μm, the breakdown path is moved to the bottom of the p-body. In this regime, the breakdown voltage decreases with increasing the depth. The effect of the width of DBC on the UIS is similar with that of the depth of DBC. It maybe noted that the depth is dominant to determine the breakdown path. The proposed device has the wide process window. When the depth and width are varied $\pm 10\%$ and $\pm 30\%$ from the optimum, the breakdown voltage is not altered much.

5. Conclusion

We propose a new power MOSFET, which improves the avalanche energy considerably, by employing a DBC. The current beneath the n+ source of the proposed device is about 20% of the conventional device. The DBC alters the direction of the current flow from the edge to the bottom of the p-body so that the possibility of turn-on of the parasitic bipolar transistor is considerable reduced. The proposed device does not require any complicated fabrication process and enjoys a wide range of the process compared with the conventional device.

References:

[1] J.Zeng et al, *ISPSD'99*, pp. 205-208, 1999.

[2] C.Kocon et al, *ISPSD'2000*, pp. 157-160, 2000.

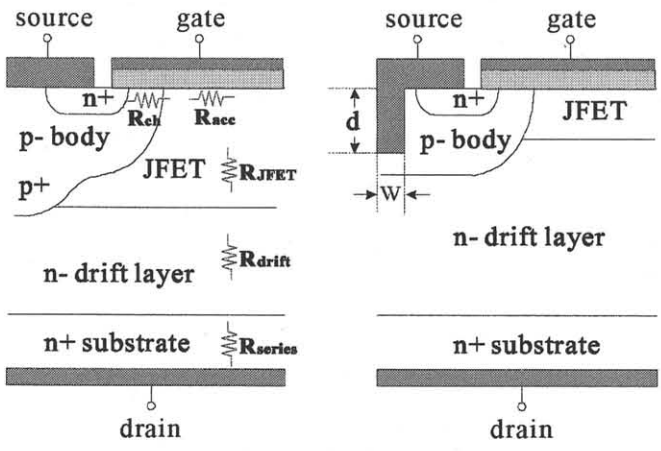
[3] R.K.Williams et al, *IEDM'97*, pp. 363-366, 1997.

[4] B.J.Baliga, Modern Power Devices, John Wiley & Sons, 1987.

[5] A.Narazaki et al, *ISPSD'2000*, pp. 377-380, 2000.

Table I. The optimized design parameters.

parameter	conventional	proposed	unit
p-body	1.5	1.5	μm
p+well	2.2	-	μm
unit cell	5.5	5.0	μm
JFET(d)	2.0	1.0	μm
JFET(c)	2.0×10^{16}	2.0×10^{16}	cm^{-3}
W (DBC)	-	0.6	μm
d (DBC)	-	1.2	μm
Nd(drift)	8.0×10^{15}	8.0×10^{15}	cm^{-3}



(a) conventional (b) proposed

Fig. 1 Cross-sectional View

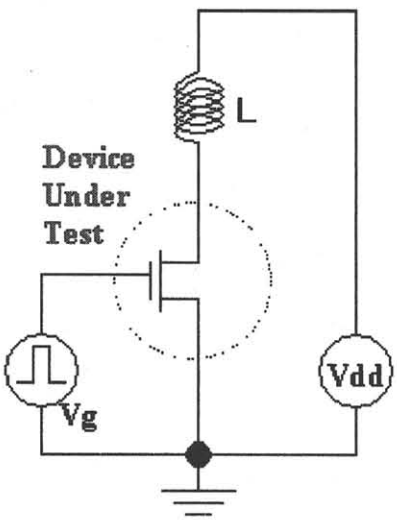


Fig. 2 Circuit diagram of UIS.

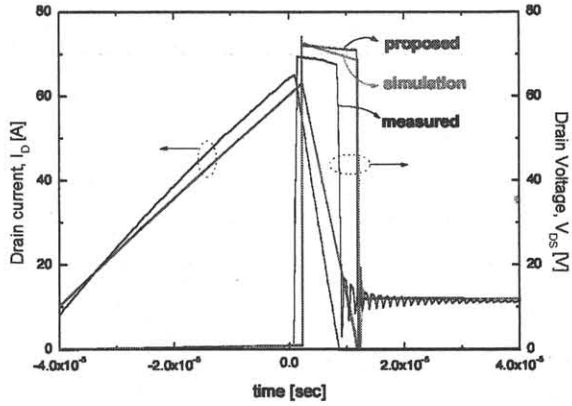
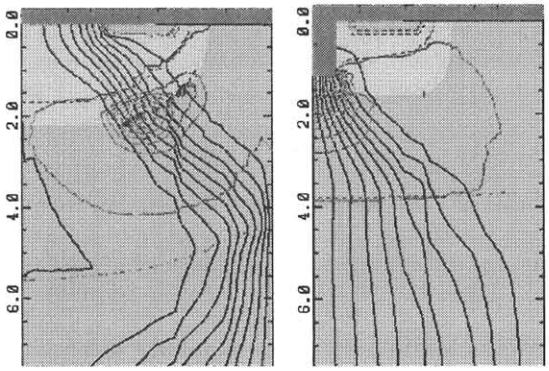


Fig. 3 Waveforms during the UIS.



(a) conventional (b) proposed

Fig. 4 Current flow and impact ionization at UIS.

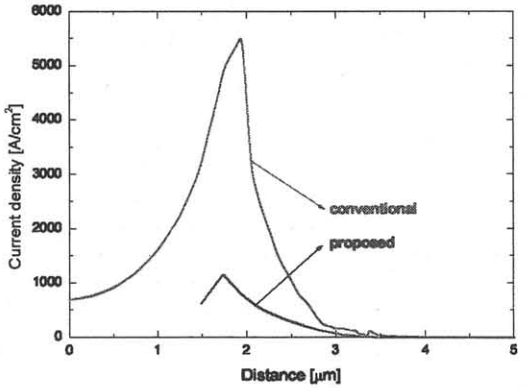


Fig. 5 Current density underneath n+ source during UIS.

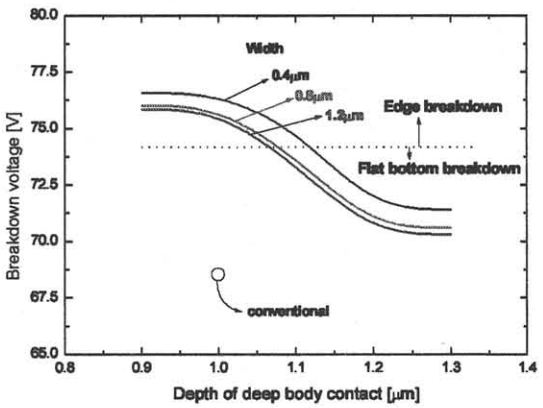


Fig. 6 Optimization of width and depth of deep body contact.