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P3-1

Annealing Effects on Interface States and Fixed Charges of $TiN/Al_2O_3/Si$ MOS structure deposited by Atomic Layer Deposition

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1. Introduction

With the continued scaling of gate length to the deep sub micron, numerous researches have been focused on high-k dielectric materials as a substitute for SiO_2 gate oxide. The candidate gate dielectrics are Ta_2O_5, Al_2O_3, HfO_2, ZrO_2 and Hf, Zr silicates, etc. Among these materials Al_2O_3 is promising since it shows a low level leakage current density due to larger band-gap although its dielectric constant is rather low. However, there are several issues to overcome for its application as gate dielectric. First, Al_2O_3 is known to have a large amount of fixed charge density [1-2] resulting in a flat band (V_{fb}) or threshold voltage shift. Second, it has a large interface state density (D_{it}) compared to SiO_2. Therefore, in this study, the variations in D_{it} and V_{fb} of $TiN/Al_2O_3/Si$ MOS capacitor with the various annealing conditions were investigated. From this investigation the optimum annealing condition was determined. "Slow" and "fast" interface states were analyzed from the hysteresis measurement of C-V curves and conductance method, respectively.

2. Experimental

5.8-nm-thick-Al_2O_3 film were grown on 8-in-diameter p-type (doping concentration of $4.7\times10^{17}/cm^3$) Si (100) wafer by an atomic layer deposition method at 350℃ using TMA (Trimethyaluminum:$Al(CH_3)_3$) and H_2O as the precursors. The growth rate of Al_2O_3 was ~1 Å/cycle. Then, 25-nm-thick TiN/300-nm-thick Al film stack was sputter-deposited as the metal electrode. The MOS capacitors with an active area of 52402μm^2 were patterned using photolithography and reactive ion etching. Post-annealing of the capacitors was performed at temperatures of 300, 375, 450℃, respectively, for 30min under H_2/N_2=10/90 ambient using a vertical furnace. For more exact comparison, one of the samples was annealed at 450℃ for 30min in N_2 ambient. The C-V measurement frequency ranged from 1KHz to 100KHz. Table 1 shows the list of annealing conditions and some data from C-V measurements.

3. Result and discussion

Fig.1 shows the conventional high frequency C-V curve of the as-fabricated sample. The measured capacitance equivalent oxide thickness (CET), from accumulation capacitance is 3.3 nm, and, thus, the dielectric constant of the Al_2O_3 film was estimated to be 6.8, which is a somewhat lower value than the bulk dielectric constant.

It is known that the hysteresis voltage (V_h) of C-V curve can be used to estimate the slow interface state density using the following equation: $N_{si}=C_{ox}V_h/q$, where C_{ox} is the areal capacitance of insulator layer and q is the electron charge [3]. The slow interface state density of the as-fabricated sample was estimated to be $1.27\times10^{12}/cm^2$, which is far higher than that of the SiO_2/Si interface. It was found that V_h was reduced with post-annealing temperature regardless of annealing ambient. Fig. 2 shows that the slow interface state density reduced to ~$3\times10^{11}/cm^2$ after the annealing at temperatures above 375℃.

It was reported that ALD-Al_2O_3 films had a large amount negative fixed charge (Q_f) of approximately $5\times10^{12}/cm^2$ and the flat-band voltage shift ($\triangle V_{fb}$) was positive. Because the fixed charge degrades device performance, it is important to understand their properties and thermal behavior with annealing conditions and to reduce their densities for device application. Fig. 3 shows that the H_2 annealing was very effective for reducing the fixed charge densities. Due to the decrease in the fixed charge, a negative voltage shift ($\triangle V_{fb}$) is obtained. The higher annealing temperature resulted in a larger $\triangle V_{fb}$. However, $\triangle V_{fb}$ was almost zero when the sample was annealed at 450℃ under N_2 atmosphere. This result suggests that there is a chemical reaction between hydrogen and the fixed charges in Al_2O_3. The reductions of fixed charge density ($\triangle N_f$) are $6.8\times10^{11}/cm^2$, $1.07\times10^{12}/cm^2$, $8.5\times10^{11}/cm^2$, of the samples annealed 300℃(H_2), 375℃(H_2), 450℃(H_2), respectively.

In order to extract fast interface state density (D_{it}), conductance of the MOS capacitors were measured as a function of frequency [4]. Fig.4 shows the change in D_{it} with annealing conditions. D_{it} of the as-fabricated sample was $1.8\times10^{12}/eVcm^2$ at the Si midgap and $1.27\times10^{13}/eVcm^2$ near the valence band edge. The D_{it} decreases with H_2 and N_2 annealing. However, no difference was observed in the 300~450℃ range. After annealing, the fast interface state density decreased to $1.4\times10^{12}/eVcm^2$ at the midgap. The capture cross-section (σ_p) near the midgap is ~6×10^{-14} cm^2 in the as-fabricated sample which is higher than that of SiO_2/Si MOS capacitor [5]. This suggests that there are higher possibility for carrier (hole) to collide with the trap centers in $TiN/Al_2O_3/Si$ MOS system.

Fig. 5 is a high resolution TEM image of sample annealed 450℃ in H_2. Al_2O_3/Si interface is very clear and no interfacial layer is observed. The TiN/Al_2O_3 interface was a little bit rough which might cause the fast state centers. More detailed study on the fast states generated by metal/Al_2O_3(or other oxide materials) system electrode will be necessary.

4. Conclusion

The variations in slow/fast interface states of $TiN/Al_2O_3/Si$ MOS capacitor as a function of the post-annealing were studied using C-V and conductance method. It was observed that the slow interface states, by fixed charge, were drastically reduced by H_2 annealing at 375℃ for 30min. Fast states were also reduced by the H_2 or N_2 annealing at temperatures higher than 300℃.

5. Reference

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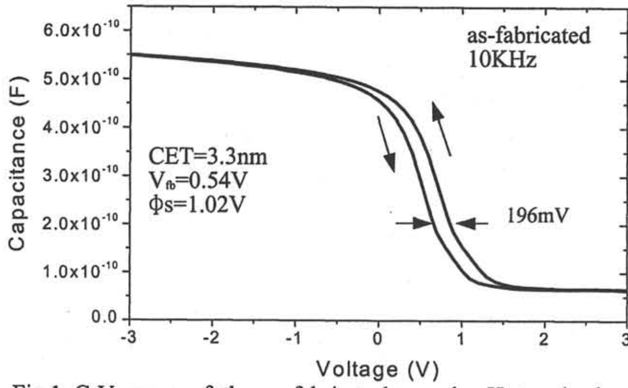


Fig.1 C-V curve of the as-fabricated sample. Hyteresis due to the slow interface states

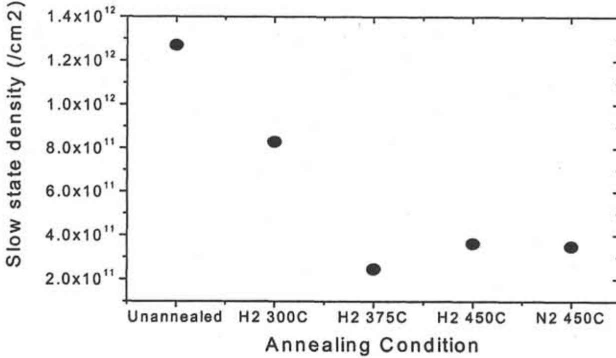


Fig.2 Slow interface states densities with annealing ondition from C-V measurement

Table I. List of samples:Annealing condition and the results of C-V measurement(10KHz).

Sample	Temp.(C)	Ambient	V_h (mV)	$\triangle V_{fb}$ (mV)
as-fabricated	-	-	169	
H_2 300C	300℃	H_2/N_2 =10/90	128	-107
H_2 375C	375℃		36	-167
H_2 450C	450℃		56	-134
N_2 450C	450℃	N_2	54	-19

V_h : Hysteresis form forward and reward voltage sweep
$\triangle V_{fb}$: Voltage shift from C-V curves due to the reduction of the fixed charge

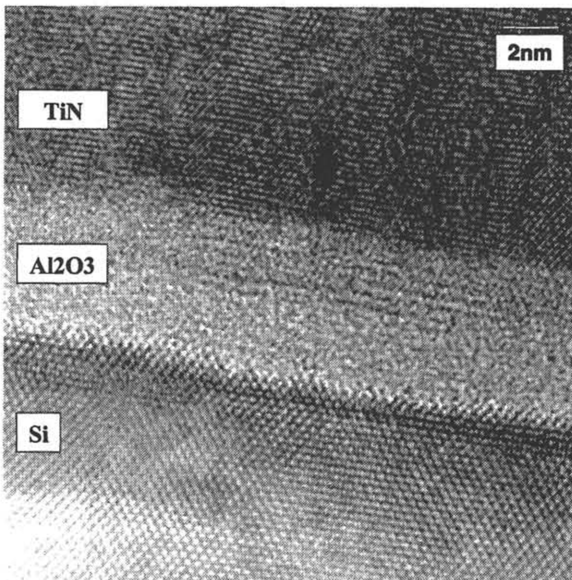
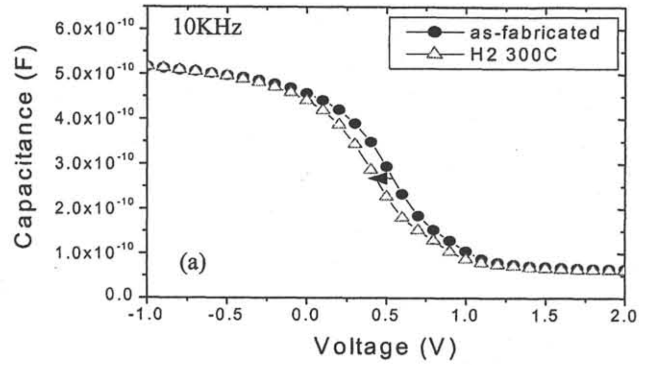
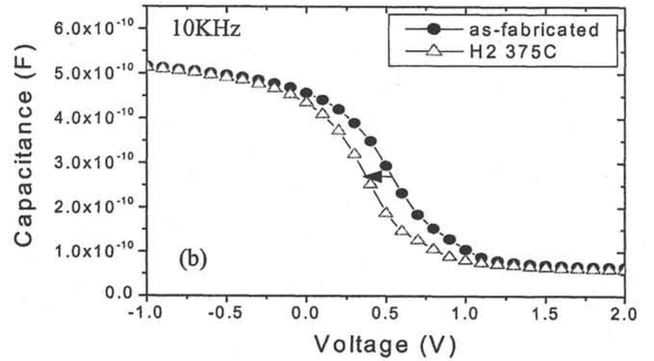


Fig.5 High resolution TEM image of the sample annealed at 450℃ in H_2. The thick of Al_2O_3 is 58Å.





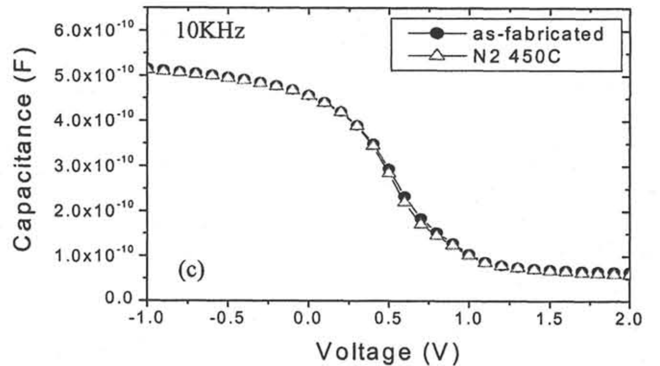


Fig. 3 The flat band voltage shift($\triangle V_{fb}$) of annealed samples from the flat band voltage(V_{fb}=0.54V) of as-fabricated sample. The negative voltage shift due to the reduction of negative fixed charge. (a) H_2 300℃, (b) H_2 300℃, (c) H_2 450℃.

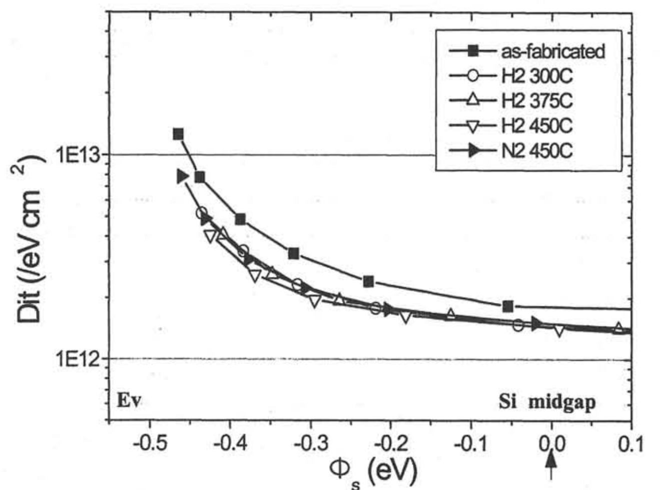


Fig. 4 Fast interface state density which obtained by using conductance method. Φs is the surface potential. (Φs=0 in Si midgap.)