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P3-10

Impact of Ti Deposition Condition and Subsequent RTA on Contact Resistance of W-Bit Line in sub-micron technology DRAM

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Introduction

Recently, as the memory density of DRAM increases, the achievement of high performance and reliability of metal interconnects of DRAM is becoming a critical concern, because both current density and RC delay time are increasing with the aggressive down scaling of cell and MOSFET's size. To meet these demands, W(tungsten) has been widely used as a bit line material due to its lower specific resistivity than conventional polycide[1]. Despite of such advantages, however, W-bit line process has some difficulties in achieving the good contact characteristics including thermal stability on the doped poly-Si plug, n+ & p+ areas and Wsix(gate) simultaneously under high thermal budget produced during the formation of capacitor in the COB(capacitor over bit line) structure[Fig.1(a)]. As W-bit line contact size becomes smaller, it is strongly demanded to obtain the good contact resistance in both cell and periphery regions, because contact resistance has the inverse proportional function of contact area[2]. In this paper, we have investigated the effect of Ti(Titanium) deposition conditions and subsequent RTA(rapid thermal anneal) on each contact resistance. And also, we propose the optimized Ti deposition condition and subsequent RTA to obtain the good characteristics of cell and periphery contact resistance simultaneously, while still keeping good other device characteristics.

Experimental

The devices were fabricated using a 0.15um technology 256M-DRAM product which is quite stable in terms of technology maturity. The key technologies used in this experiment were summarized in Table 1. In order to verify how Ti thickness with different Ti deposition conditions and subsequent thermal treatment affect each contact resistance of W-bit line, two sample groups were prepared [Table 2]. Group-1 was manufactured to investigate the effect of Ti thickness at fixed TiN200 Å and subsequent RTA 845℃(for fixed 20sec in N_2 ambient) and Group-2 was fabricated to find out the effect of Ti deposition condition and subsequent RTA temperature on each contact resistance of cell and periphery regions. Especially, the optimized barrier metal condition of W-bit line was proposed in Group-2 and characterized by the wafer uniformity of each contact resistance for all splitting conditions. In addition, we evaluated the tDPL(data-in to prechage time) characteristics closely related to cell contact resistance and data retention time characteristics associated with thermal treatment[3] in memory cells, practically.

Results and Discussion

Fig.1(b) and (c) show the TEM images of TiN/$TiSi_2$ using direct W-bit line contact to poly plug, n+ and p+ active areas which are very sensitive to the barrier metal thickness and subsequent thermal treatment. In Fig.1(d), schematic diagram of critical cell contact area closely associated with tDPL characteristics is illustrated. For better tDPL margin, bit line contact as well as storage node contact to poly plug resistance should be reduced, simultaneously. In Fig.1(e), the practical tDPL failure rate increases as the bit line contact to poly plug Rc increases. And also, it is well-known that BLC(bit line contact) to n+ and p+ Rc of transistors are directly related to the driving ability of n/pMOSFET in periphery circuits. First, Fig.2 represents the Ti thickness dependence of each contact resistance in cell and periphery areas, respectively. As the deposited Ti thickness goes up, both BLC to poly plug Rc and p+ Rc increase, while BLC to n+ Rc decreases. As shown in SIMS profile of Fig.3, the reason of BLC to poly plug Rc increase was revealed that the decrease of the phosphorous concentration in $TiSi_2$ formation area on poly-Si plug due to the increase of out-diffusion of phosphorus to TiN/$TiSi_2$ layer, as the actual-deposited Ti thickness increases. And BLC to p+ Rc increase resulted from the high boron consumption in the doped Si layer during silicide formation[4]. On the contrary, we believe that BLC to n+ Rc decrease was because of the decrease of $TiSi_2$ sheet resistance as Ti thickness increases[Fig.4], even though n+ contact area still has the agglomeration of $TiSi_2$ [Fig.7 (a)&(b) in n+ Rc area]. In order to minimize the trade-offs of each contact resistance in cell and periphery regions, we investigated the effect of the optimized Ti deposition condition including a moderate Ti thickness and a subsequent RTA process on each contact resistance. As shown in Fig.5, compared to conventional(Con, ~20mTorr) condition, low pressure(LP,~5mTorr) Ti deposition condition is very efficient to improve all bit line contact resistance characteristics concurrently. That is because LP condition can effectively control the thicker Ti on the bottom side(Fig.5(b)-①) and the better side step coverage(Fig.5(b)-②) inside contact hole by reducing the straight direction than conventional condition, resulting in improving the uniformity of Ti thickness in contact hole area as well as obtaining the same Ti thickness as conventional condition. In Fig.6, after subsequent RTA 845℃, BLC to n+ Rc of LP-Ti80 Å condition was reduced 20% compared to that of Con-Ti60 Å, while BLC to poly plug Rc and p+ Rc slightly decreased. And also, it was observed that the subsequent RTA temperature control above critical value is very useful to get rid of the agglomeration on contact area generated during $TiSi_2$ formation[Fig.7(c)] as well as to reduce the $TiSi_2$ sheet resistance[Fig.8]. By applying RTA 865℃ based on Con-Ti60 Å, BLC to poly plug Rc, n+ Rc and p+ Rc are reduced about 33%, 45% and 14% respectively, compared to that with RTA 845℃[Fig.6]. Consequently, we found out that BLC to poly plug Rc, n+ and p+ Rc characteristics could be dramatically reduced simultaneously using LP-Ti80 Å/RTA865℃ without any trade-off of other device characteristics such as n+/PW & p+/NW junction leakage in periphery region[Fig.10] and the data retention time in memory cells[Fig.12]. Especially, as shown in Fig.9, we observed that the in-wafer uniformity characteristics of BLC to n+ Rc using the proposed condition(LP-Ti80 Å/RTA865℃) represents the excellent improvement effect compared to that using the conventional condition(Con-Ti60 Å/RTA845℃). In addition, BLC to poly plug Rc characteristics by applying the proposed condition was improved around 50% compared to that of conventional condition, resulting in reducing the tDPL failure rate(around 12%) in memory cells as shown in Fig.11.

Conclusion

We have intensively investigated the impact of Ti deposition condition along with optimal Ti thickness and subsequent RTA temperature on each contact resistance of W-bit line. And we found out that low pressure(~5mTorr) Ti deposition condition with the subsequent RTA temperature above critical value is very useful to improve the uniformity of Ti deposited thickness inside contact hole and to remove the agglomeration on contact area, resulting in the excellent improvement of W-bit line contact characteristics. In particular, the optimized condition(LP-Ti80 Å/RTA865℃) suitable to 0.15um DRAM technology and beyond is proposed in order to obtain the good contact resistance of cell and periphery areas simultaneously, while still keeping good other electrical properties.

References

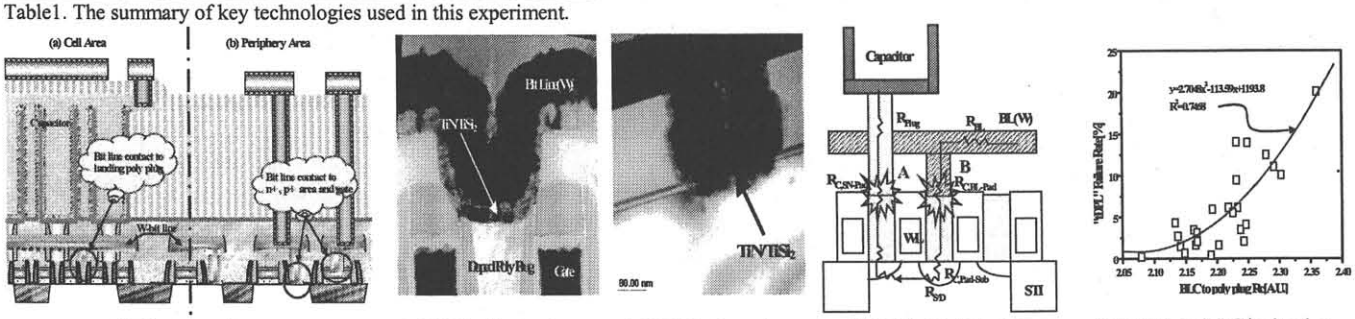
[1]. H.K.Kang, *et al.*, IEEE, IEDM Tech. Dig. 1994, p635
[2]. B.J. Jin, *et al.*, IEEE, VLSI Tech. 2001, p127
[3]. D.C.Kim, *et al.*, IEEE, IEDM Tech. Dig. 2001, p18.3.1
[4]. I. Asano, *et al.*, SSDM, 2001, p30

Memory cell structure	**Capacitor Over Bit line(COB)**
Design Rule	**0.15㎛**
Isolation scheme	**Shallow Trench Isolation(STI)**
Gate stack layer	**Wsix/Poly-Si/SiO_2**
Cell landing poly plug	**Poly plug formation by CMP**
Bit line layer	**Tungsten(W) by Direct W scheme**
Cell storage node contact	**Self Aligned Contact(SAC)**
Cell capacitor dielectric	**NO**
Metal layer	**Al (2 metal layers)**

Table1. The summary of key technologies used in this experiment.

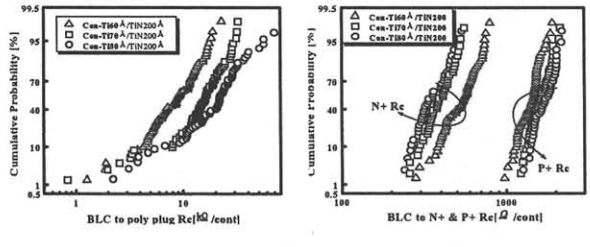
Split Group	Ti Thickness[Å]@TiN=200 Å / Subsequent RTA[℃]	Ti Deposition Condition
Group-1 (Lot #1)	Con-Ti 60 / RTA 845 Con-Ti 70 / RTA 845 Con-Ti 80 / RTA 845	*Con- : Conventional =~20mTorr
Group-2 (Lot #2)	Con-Ti 60 / RTA 845 Con-Ti 60 / RTA 865 LP- Ti 80 / RTA 845 LP- Ti 80 / RTA 865(Proposed)	*LP : Low pressure = ~5mTorr

Table 2. The splitting conditions of Ti thickness with different deposition methods and subsequent RTA to verify the effect of Ti thickness and the thermal treatment for ohmic contact formation on each contact resistance in cell and periphery areas. Especially, the optimized barrier metal condition of W-bit line with subsequent RTA temperature was proposed in Group-2.



(a) Cross-section (b) BLC/poly plug (c) BLC/n+ or p+ (d) Cell contact area (e) tDPL vs BLC/poly plug

Fig.1 (a) The view of cross-section in cell and periphery areas of DRAM with COB structure. TEM image of direct W-bit line contact to poly plug(b) in cell and n+ or p+ area(c) in periphery areas, which are sensitive to barrier metal thickness and subsequent RTA. (d) Schematic illustration of critical contact area closely related to tDPL characteristics in memory cell. Bit line contact[B]as well as storage node contact[A]to poly plug resistance should be reduced, simulatneously. This is because the accurate voltage transferring is impossible for giving efficient charge to storage node due to voltage drop across the cell contact resistance of A and B areas. (e) The practical tDPL characteristics is shown with increasing the bit line contact to landing poly plug resistance.



(a) Cell Area (b) Periphery Area

Fig.2 Cumulative probability of BLC to poly plug Rc in cell region and BLC to N+ Rc & P+ Rc in periphery area for each splitting condition in Group-1.

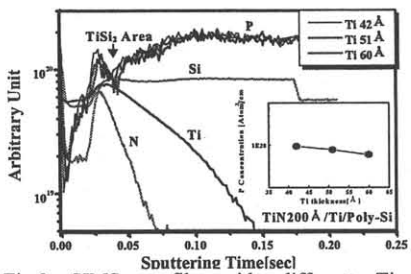


Fig.3 SIMS profile with different Ti thicknesses of TiN/Ti/poly-Si area in cell region after RTA 845℃.

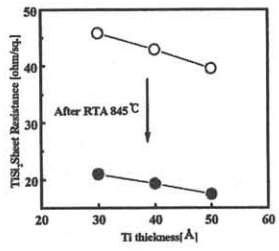
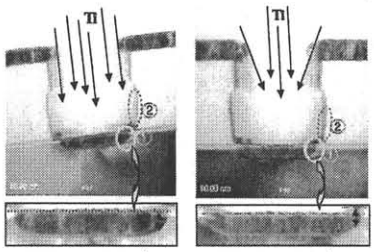
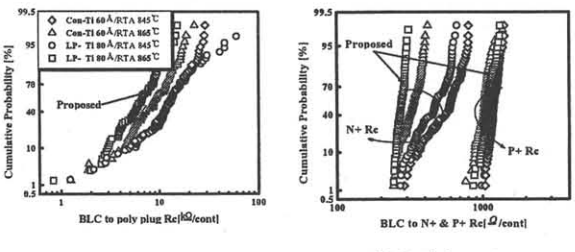


Fig.4 $TiSi_2$ sheet resistance[Rs] characteristics with different Ti thicknesses in BLC to n+ Rc area.



(a)Con-Ti 60 Å (b) LP-Ti80 Å

Fig.5 Comparison of Ti deposition condition. Con-: ~20mTorr, LP:~5mTorr



(a) Cell Area (b) Periphery Area

Fig.6 Cumulative probability of BLC to poly plug Rc in cell region and BLC to N+ & P+ Rc in periphery region to obtain the effect of Ti deposition condition and subsequent RTA in Group-2.

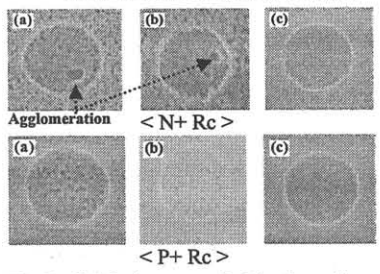


Fig.7 SEM image of Ti deposition condition with subsequent RTA.
(a) Con-Ti 60 Å / 845℃, (b) LP-Ti 80 Å / 845℃ and (c) LP-Ti 80 Å / 865℃

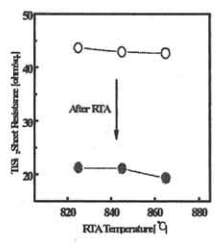


Fig.8 Sheet resistance of $TiSi_2$ with subsequent RTA temperatures in BLC to n+ Rc area.

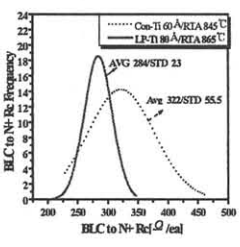


Fig.9 Frequency dirtribution of BLC to n+ Rc area in wafer for splitting conditions.

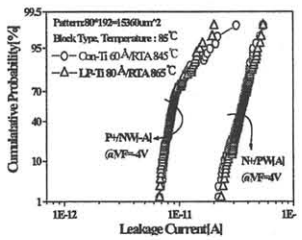


Fig.10 Comparison of N+/PW and P+/NW junction leakage in each wafer.

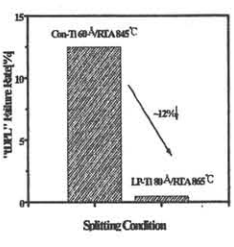


Fig.11 Characteristics of "tDPL" failure rate for splitting conditions.

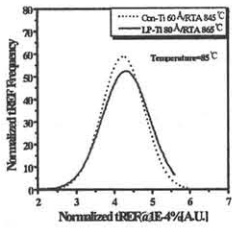


Fig.12 Frequency distribution of normalized data retention [tREF@1E-4% failure rate] in memory cells.