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SOI/Bulk Hybrid Wafer Process Using SEG (Selective Epitaxial Growth) Technique for High-End SoC Applications

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1. Abstract

SOI/Bulk hybrid wafer, which has both SOI regions and bulk regions, to embed both SOI device and trench capacitor memory cells in same chip was developed. Partial etching of SOI/BOX (Buried OXide) layers and SEG (Selective Epitaxial Growth) process simply transform an SOI wafer into a high quality SOI/Bulk hybrid wafer. Silicon nucleation on the mask region was systematically investigated. It was proved that nucleation could be suppressed with appropriate deposition condition and mask size. The property of trench capacitor memory cells fabricated in bulk region of SOI/Bulk hybrid wafer was comparable to those for a bulk wafer.

2. Introduction

Recently, demands for the embedded DRAM have been increasing rapidly, which brings about high bandwidth between memory and logic with low power consumption and reduced chip size. However, embedding of DRAM in the SOI wafer is problematic, because DRAMs on SOI wafer can suffer from deterioration in data retention and data sensing owing to so-called floating-body effect [1-3]. In order to solve the problems device fabrication with SOI/Bulk hybrid wafer comprising both SOI substrate regions for SOI logic and bulk regions for bulk-structured DRAMs is an attractive method.

There have been demonstrations using the SOI/Bulk hybrid wafer produced by SIMOX process [4,5]. However it has fundamental issue that dislocations are inevitably formed at the edge of BOX region because of the stress due to the oxygen implantation. In this paper, SOI/Bulk hybrid wafer using SEG process is reported. The issue of this process is the suppression of silicon nucleation on mask region.

3. Fabrication of SOI/Bulk hybrid wafer

Fig.1 shows the device structure on SOI/Bulk hybrid wafer. Parts of SOI layers were covered with SiN and then Si was grown selectively on the base substrate exposed by etching SOI/BOX layers. The epitaxial layer thickness was about 0.2~0.4μm which is equal to the summation of SOI and BOX layer thickness.

4. Robust design for selective epitaxial growth

4-1. Dependence of silicon nucleation on deposition condition

Fig.2 shows the silicon nucleation on a wafer covered with SiN layer under various process conditions. The silicon nucleation increased as the growth rate increased, and the critical growth rate was about 0.4μm/min. It is thought that silicon nucleation was increased because of the increasing of the density of silicon atoms on the SiN layer. Increase of the substrate temperature and decrease of the HCl flow rate tend to occur silicon nucleation.

4-2. Design of the mask size for SOI/Bulk hybrid wafer

Mask area, according to tip design, occupies 30 - 70% of chip, which has several cm square areas. The process margin for SEG can be widen by designing of mask region.

Fig.3 shows the schematic illustrations of SiN patterned mask samples. The sample has square SiN mask region with a side of 15mm, 22.5mm and 30mm. The SEG regions had the same size as the mask size. Silicon nucleation was detected by Particle counter and SEM. The dependence of silicon nucleation on deposition time was investigated by three kinds of mask area and shown in Fig. 4. The coverage ratio is defined as the silicon-nucleated area versus remaining SiN mask area calculated from SEM photographs. The difference was the time when silicon nucleation takes place.

Fig.5 shows the dependence of the incubation time before silicon nucleation on mask area. Silicon nucleation can be suppressed by decreasing mask area.

It is thought that the time until the threshold density of silicon atoms to form nuclei is longer on small mask area than large one, because an atom on small mask fall out of mask easier than on large one. Rectangle mask should be used for getting the margin of selectivity more than square mask, because silicon atoms on mask region fall out easily on short side.

With sufficiently small mask pattern, silicon nucleation can be completely suppressed. Fig.6 indicates that nucleation never occur near the mask edge. The distance of the nucleation free region can be estimated as shown in Fig.7. It is surmised that the distance of silicon nucleation-free from mask edge is 1.4mm under this deposition condition.

5. Fabrication of MOS device on SOI/Bulk hybrid wafer

Fig. 8 shows wafer bitfail maps of 1 Mb trench capacitor memory cells [6]. Bulk and SOI/Bulk hybrid wafer attained the same high yield of 90 %. The data retention characteristics perfectly coincided with each other in both the main-mode and the tail-mode regions, which have never been presented in the previous work.

6. Conclusion

SOI/Bulk hybrid wafer process was developed. Extensive investigation of chip design as well as deposition condition revealed that robust process could be realized for SOI/Bulk hybrid wafer.

References

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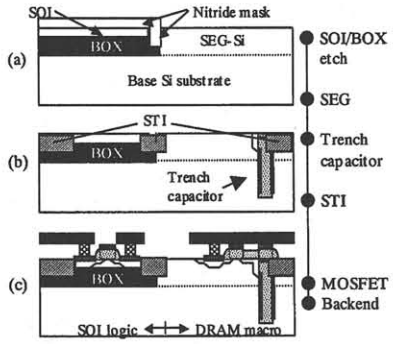

Fig.1. Device structure on SOI/Bulk hybrid wafer.
(a) SOI/Bulk hybrid wafer formation.
(b)(c) SOI Logic and DRAM macro are formed with embedded DRAM process.

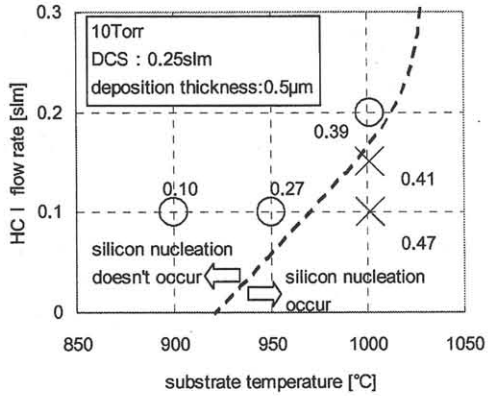

Fig.2. Silicon nucleation on SiN layer at various process conditions. The circle indicates that nucleation does not occur and the cross indicates that nucleation occurs. The silicon nucleation is enhanced as the growth rate increases. The dashed line indicates the critical growth rate of about 0.4μm/min.

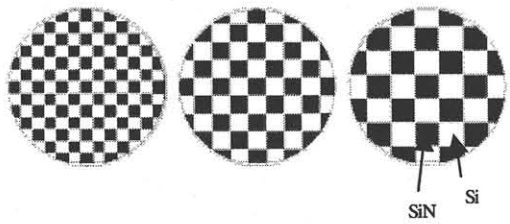

Fig.3. Schematic illustration of SiN patterned mask sample.
Each sample has square SiN mask region with a side of 15mm, 22.5mm and 30mm. The size of SEG region was the same to mask size.

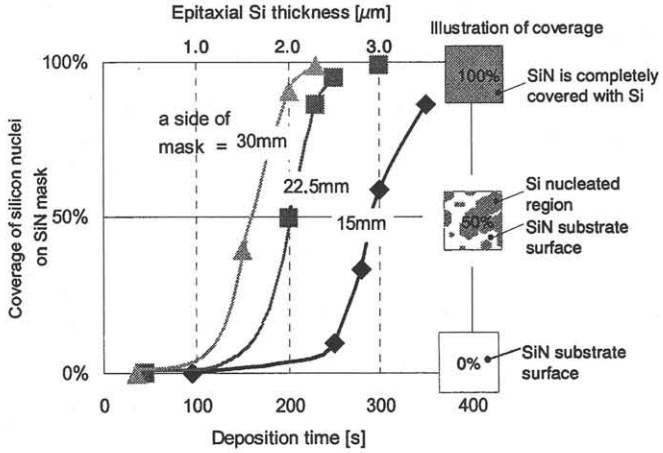

Fig.4. Coverage of silicon nucleated region on SiN mask as a function of deposition time. Incubation time before nucleation depends on mask size. Deposition condition was 1000°C, 10Torr, DCS/HCl=0.25/0.10slm.

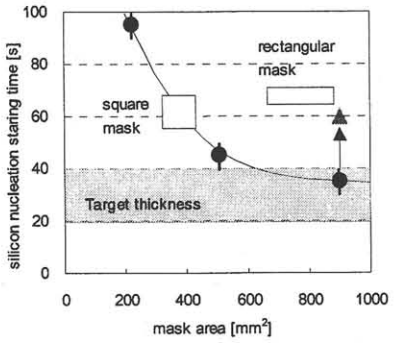

Fig.5. Incubation time as a function of mask size under the deposition condition shown in Fig.4. Long incubation time was obtained with small size of mask. Rectangle mask is preferred for much longer incubation time.

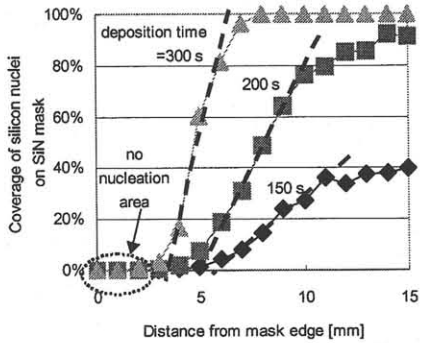

Fig.6. Coverage of silicon nuclei on SiN mask as a function of distance from mask edge for various deposition times. Silicon nucleation never occurs near the mask edge. Deposition condition is 1000°C, 10Torr, DCS/HCl=0.25/0.10slm, 150s (1.5μm)~300s (3.0μm), and the mask area is 30mm.

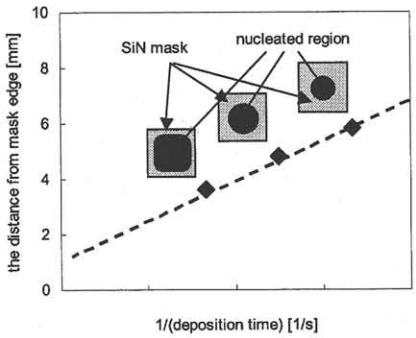

Fig.7. Nucleation-free distance from the mask edge at various deposition times on 30mm-pattern. By extrapolating the line to the y-axis, nucleation-free distance from mask edge can be estimated 1.4mm, even if the deposition time is too long.

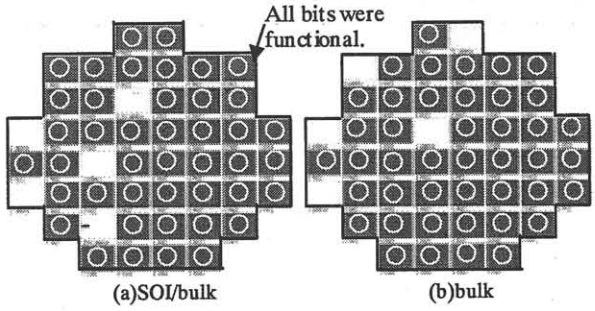

Fig.8. Wafer bitfail maps of 1Mb ADMs in the same lot.
○ indicates perfect ADM (all bits were fully functional).
Both wafers attained perfect ADM yield of 90%. There are few fail bits indicated by black dots in fail ADMs.