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One Cleaning Solution for Complete CMOS Processes

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Introduction

The RCA cleaning processes has been used more than 30-year [1], it is still used in the CMOS production line. There are two-step in RCA cleaning process, including NH_4OH : H_2O_2: H_2O (SC-1) to remove particles and some trace metallic contamination, and HCl: H_2O_2, H_2O (SC-2) to remove metallic contaminants. When wafers undergo the photoresist (PR) patterning, an additional step of H_2SO_4: H_2O_2 (SPM) should be added to remove the residual PR. Figure 1 shows a typical cleaning process in a deep-sub-quarter-micron CMOS fabrication. Before silicidation, there are 19 cleaning-step and 4 different cleaning methods. Where clean-A is the RCA plus SPM, clean-B is the RCA, clean-C is for SPM only, clean-D is for pre-gate oxide cleaning. It is noted that, the number of cleaning steps in the CMOS fabrication is huge and cleaning method is complex.

Hence, the purpose of this study is to develop one cleaning solution to replace all cleaning methods mentioned above. At the same time, the cleaning efficiency and the final devices' performance can be still maintained. In our previous reports, such a cleaning solution has been successfully employed in post-CMP cleaning on poly-Si polishing [2], in pre-gate oxide cleaning [3], and finally optimized the recipe in pre-gate oxide cleaning [4]. The one cleaning solution bases on the conventional SC-1 with addition of tetramethyl ammonium hydroxide (TMAH), a surfactant to enhance particle removal efficiency, and ethylenediamine tetraacetic acid (EDTA) to reduce metallic contamination. The optimized temperature is 60°C and time is 5-min.. On the other hand, it is 70°C and 10-min. for RCA. We have demonstrated the good efficiency for removing particles, metallic contamination and organic. It demonstrated the comparable or even better performance than two-step RCA cleaning processes [2-4]. Consequently, this is the first time, we extend this recipe to complete CMOS fabrication process. We found this scheme shows very significant improvement and advantages.

Device Fabrication

There are two splits of nMOSFETs in our study. One is underwent conventional RCA cleaning process as shown in Fig.1, the other was cleaned by one cleaning solution only for every cleaning step, i.e., the step in clean A to clean D was replaced by this one-cleaning solution. The step is only one and DI water rinse time is only one too. After LOCOS isolation, wafers were implanted for Vth adjustment and anti-punchthrough. The gate oxide thickness was 3.2 nm and poly-Si gate is 200 nm. After S/D implant, wafers were annealed by RTA at 1050°C for 20-sec.

Results and Discussion

Figure 2 shows the Id-Vd curves for a long channel device (L= 250 μm). Device with one-cleaning solution (one-step) exhibits 4.6 % higher driving current than RCA counterpart (control) @Vg-Vt=3 V and Vd=3V. As channel length is 1-μm, the improvement increases to 7.7%, (not shown). Transconductance at linear region for L=250 μm are shown in Fig.3. Improvements are 6.8 %. The transconductance for 1-μm device shows the same trend as those for long channel devices. Larger improvement (~18.4%) at G_{mmax} is found. This is due to cleaner and flat interface can be obtained by one-step cleaning [2-4]. One-step devices also have better performance in interfacial defect density, D_{it}, (2.22×10^{10} $cm^{-2}eV^{-1}$, and 5.07×10^{10} $cm^{-2}eV^{-1}$ for control) sub-threshold swing (80.2 vs. 81.7 mV/dec.).

Figure 4 shows the gate leakage at 1.0V for the MOS capacitors. It is almost the same level for both samples. Breakdown field distribution is shown in Fig. 5. One-step devices show even better performance than control ones. Time-to-soft breakdown is also measured and shown in Fig. 6. They are comparable. To confirm this result, a second run was performed. The driving current is still improved for one-step devices for both L= 1, and 250 μm. Figure 7 compares the DI water consumption and processing time for both methods. For one CMOS lot, it saves 20-times DI water rinse by using one-step solution. The typical time-saving for cleaning is around 9 hours for each lot. The overall benefits for this process are compiled in Fig.8. They are: reduced cost of equipment to 1/3; and time for each cleaning process to 1/2 to 1/3; reduced DI water consumption. Take a 30,000 wafer/month line for example, around 1200 lots, it saves DI water as high as 1200x20x300 liter, 7.2×10^6 liter/month, where 300-liter is the typical DI consumption for one 8-in lot for one rinsing cycle. Since the time for each run can be reduced at the same time, the throughput can be increased simutaneously. But the most important is that we don't need to handle huge chemical waste as before, it is of great benefit to our environment eventually.

References

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High Performance Logic Flow

1. Initial clean
   - H_2SO_4/H_2O_2 (10-min) — Clean A
   - H_2O (10-min)
   - SC-1 ($NH_4OH/H_2O_2/H_2O$) (10-min)
   - H_2O (10-min)
   - SC-2 ($HCl/H_2O_2/H_2O$) (10-min)
   - H_2O (10-min)
2. Zero-layer:
   - SC-1 (10-min)
   - H_2O (10-min)
   - SC-2 (10-min) — Clean B
   - H_2O (10-min)
3. N-well I/I: clean A
4. P-well I/I: clean A
5. Define PBLOCOS: clean A
6. N-field I/I: clean A
7. Oxidation: clean B
8. Strip (pad oxide): clean B
9. Strip oxide: clean B
10. P, N-anti and V_{th} I/I: H_2SO_4 only — Clean C — twice
11. Pre-gate oxide: H_2SO_4, O_3, Vapor HF/H_2O — Clean D
12. Poly-Si etching: clean A
13. N-LDD, P-LDD:clean C: twice
14. Spacer: clean A
15. N^+ S/D, P^+ S/D: clean C twice
16. Pre-silicide: clean A

Total: clean A: 8 clean B: 4 clean C: 6 clean D: 1

Fig.1 The cleaning steps in conventional CMOS process.

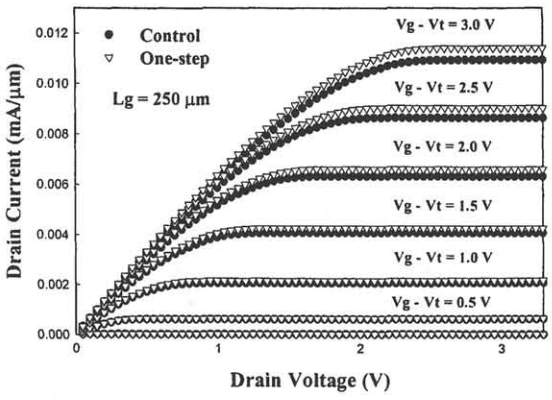

Fig.2 Id-Vd curves for L=250 μm devices.

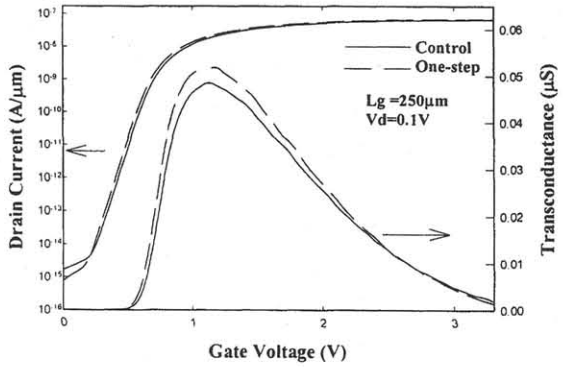

Fig.3 Transconductance for L= 250 μm at linear region.

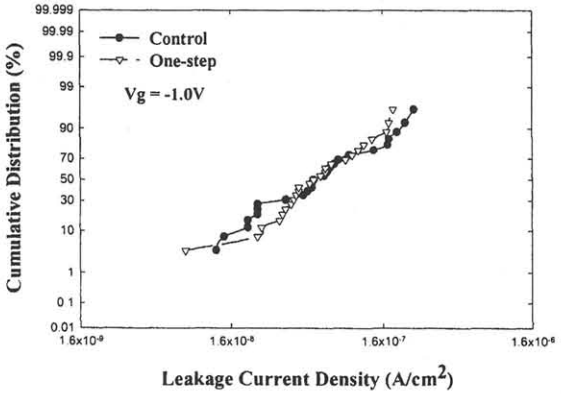

Fig.4 Gate leakage of MOS capacitor of area $9x10^{-4}$ cm^2.

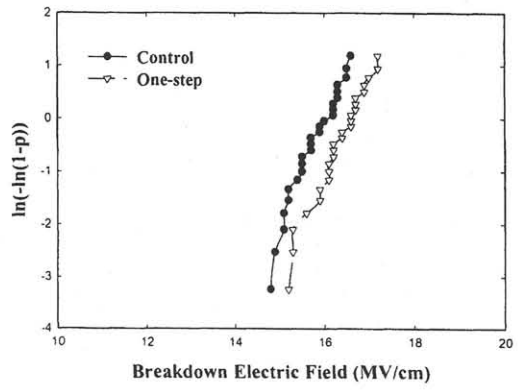

Fig.5 Distribution of breakdown field

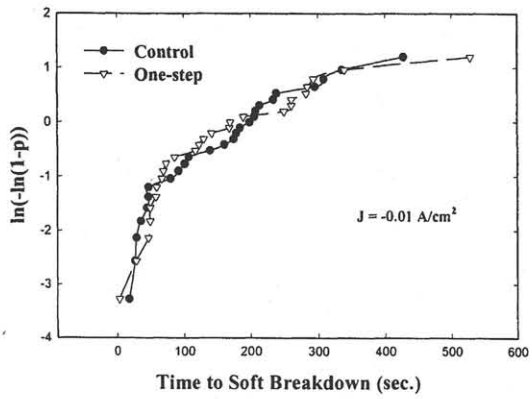

Fig.6 Distribution of time-to-soft-breakdown.

RCA vs. One-Solution

Times of H2O-rinse by RCA	Times of H2O-rinse by One-solution	Difference	Total # in CMOS	Number saved
A: 3	1	2	8	16
B: 2	1	1	4	4
C: 1	1	0	6	0
D: 1	1	0	1	0
Total				20

- Time
- ***RCA:***
  - Clean A:60-min
  - Clean B: 40-min
  - Clean C: 20-min
  - Clean D: 50-min
- ***One-solution:***
  - Clean one: 15-min
- ***Save***: 8.75-hour

Fig.7 D.I. water rinse times for RCA and one-step solution.

	RCA	One-solution	Remarks
Cost of Equipment	Expensive Foot print	Cheap (<1/3) Less area Good for mini-fab.	Only one bath
Time of cleaning process	Long	Short (<1/2)	average
Cost of H_2O, chemical, waste-handling	High	For 30000/month (1200 lots), it saves 1200x20x300 liter=$7.2x10^6$ liter/month	20-time H2O saved in CMOS, 300-liter for one cleaning step in 8-in bath
Time of each run	long	Short	Save 8.75 hours for each lot

Fig.8 Merit of one-step solution vs. RCA cleaning method.