Low Power CMOS Process Technologies and Characteristics for advanced High Density Mobile DRAM

Chi Hoon Lee*a, Nam Hyuk Jo, Dong Gun Parkb, Duk Dong Kang, Dong-Ho Ahn, Chan Seong Hwang, Tae Sung Kim, Hyeong Joon Kim, and wonshik Lee

*aSchool of Materials Science & Engineering, Seoul National University, San 56-1, Shillim-dong, Kwanak-ku, Seoul, KOREA
bDRAM Process Architecture Team, Process Development Team, Memory Product & Technology Division, Samsung Electronics Co., Ltd., San3842, Nongseo-Ri, Hweunge-Eup, Yongin-City, Kyungki-Do, KOREA

Phone:82-2-880-5451(233), Fax: 82-2-887-6575, E-mail:chi2000@smc.ac.kr

I. Introduction

A new fabrication process is required to produce high density (2-128M) low power DRAMS for mobile equipment. Therefore, a decrease in the gate oxide thickness in the logic area for a larger current and an increase in the gate oxide thickness in the cell array for a longer cell array refresh time is considered to be the optimum process. For this reason, a dual gate oxide (DGOX) process was adopted [1,2]. Preliminary reports show the gate oxide thinning effects of a shallow trench isolation (STI) active edge and other parameters [3,4]. In this paper, a low power DRAM (Vcc=1.8V) with a sub-0.17μm fabrication process and superior performance characteristics to a conventional DRAM (Vcc=3.3V) was used. The remaining oxide was decreased by wet etching before the STI gap fill process was used to release the STI top edge stress-induced leakage current [3,5]. The optical proximity correction (OPC) was used to decrease the gate oxide thickness according to the pattern loading effect, and the boron channel dose control was used to correct the electrical parameters (Vth, Id, BV, etc.).

II. Experimental

Fig. 1 illustrates the front-end key process steps for the low power DRAM with a dual gate oxide. CMOS with SGOX and DGOX were fabricated with a 0.17μm cell array and a minimum 0.26μm in the periphery area using a polycide gate CMOS process, having 6.5nm pure SiO₂ dry oxide in the conventional SGOX samples and 7.8nm (in the cell and high Vcc periphery) /5.0nm (in the core and periphery) pure SiO₂ dry oxide in the DGOX ones. Boron channel implantation into the substrates at 30-40KeV through a screen oxide layer was done to optimize the transistor performance. The first gate oxides were grown in the 6.5nm pure SiO₂ dry oxide at 850°C in the DGOX samples. However, 2.3-8.0nm pure SiO₂ dry oxide was used in the samples. The second oxide, a region of thin (5.0nm) and thick (7.8nm) gate oxides was separated by an additively patterned wafer to expose the thin oxide region, BOE etching was used to produce the first oxide, and second pure SiO₂ dry oxide (5.0nm) was grown at 850°C. After patterning the polycide gate, a SiN₂ spacer was formed for the lightly doped drain (LDD) and the rapid thermal annealing (RTA) at 980°C for 10 seconds was used for the As⁺ activation of the nmos source/drain junction with a 3.0x10¹⁵/cm² dose for nmos. Finally, P⁺ ion implantation was done with 5.0x10¹⁵/cm² for the pmos. The transistor characteristics were measured with a HP4156 and the vertical structure was examined using TEM analysis. Fig. 2 shows the process flow of the dual gate oxidation and STI top edge rounding. The second oxidation could also be grown with dry oxidation because the smoothly curved active corner increased by over 10% in edge oxide thickness, which improved the productivity.

III. Results and Discussion

Fig. 3 shows a TEM image of the STI top edge profile after growing the second oxide with or without a pad-oxide undercut. The STI active corner with the pad-oxide undercut was very smooth compared to the case without. The wet etching (LAL chemical) time was in the range of 30-50 seconds and the lateral length of the pad-oxide undercut was approximately 15nm and the thickness was approximately 10nm. the curvature of the leakage current in the 32M cell array as a function of the breakdown field was similar in the sample, but the DGOX cell array decreased by approximately 1V (4.6%) compared to the other samples, as shown in Fig. 4. The curvature of the leakage current as a function of Vg was also similar between the samples and the leakage current decreased by approximately 1.3V (15%) with increasing gate oxide thickness and applying pad oxide undercut treatment, as shown in Fig. 5. This suggests that the thickness oxide quality of the DGOX slightly decreases relative to that of the SGOX due to dual oxidation. However, the leakage current decreased with increasing thick oxide thickness of the DGOX. Fig. 6 shows the cumulative distribution of the gate oxide thickness as a function of current density increase [6]. SGOX and DGOX were used for the samples, and the STI top oxide was removed by wet etch in the SGOX region. Therefore, the leakage current was reduced by approximately 12% at a similar Vth of the SGOX due to a decrease in the gate oxide thickness. The Vth and ION of DGOX nmos with the thick oxide increases and decreases to approximately 40% (Vth: 0.65V-0.85V, ION: 85mA-120mA) compared to that of the thin oxide. Fig. 8 shows the GIDL current of the cell array with the Vcc. The GIDL current decreases 50% and the cell channel boron dose decreases 7% for the same cell Vth due to the increase in the gate oxide thickness (6.5nm-7.8nm, 20%). The refresh characteristics of the DGOX samples were improved by a decrease in the GIDL current, a decrease in the electrical field due to the decrease in the boron dose, and STI top corner stress relief. The refresh failure of the DGOX samples was observed at lower fields than that of the SGOX due to reasons previously stated, as shown in Fig. 9. The refresh time of DGOX samples was approximately 350-400msec and improved over 15% in the DGOX samples. Fig. 10 shows that the nmos hot carrier immunity (HCI) characteristics of the DGOX sample were comparable to the SGOX due to the oxide cleaning optimization.

IV. Conclusion

The process of a wet etching for pad-oxide undercut to smooth the STI active top edge and dual gate oxidation due to an improvement in MOSFETs performance for a low power (Vcc=1.8V) DRAM was investigated. A combination of these processes greatly improved the saturation current, the leakage current, and the refresh characteristics. Therefore, the gate oxide in our DGOX process was all grown under dry oxidation, which improved the productivity. Nmos HCI characteristics of the DGOX samples were comparable to the SGOX due to the oxide cleaning optimization.

V. Reference

STI isolation with or w/o pad oxide undercut 10nm screen oxide
Channel adjustment ion implantation
Screen oxide strip
DG0X photo to close cell array for thin oxide(7.8nm) and to open core and periphery for thin oxide(3.0nm)
2nd gate oxidation (pure dry SiO2, 5.0nm)
Gate poly silicon patterning with optical proximity correction method
α-implantation(120kHz)
side wall spacer(SiN) length optimization

Fig. 1 The front-end key process steps for low power DRAM with dual gate oxide. The gate oxide thickness of Conventional DRAM is 6.5nm and that of low power DRAM (DG0X) is 7.0nm and 5.0nm in the thick and thin region, respectively.

(a) TEM and VSEM images of STI top edge profile after the second oxidation. (a) STI corner round of active with wet etching for pad oxide undercut is smooth, (b) and very steep in the case without wet etching for pad oxide undercut.

Fig. 3 TEM and VSEM images of STI top edge profile after the second oxidation. (a) STI corner round of active with wet etching for pad oxide undercut is smooth, (b) and very steep in the case without wet etching for pad oxide undercut.

(a) SOG0X 5.0nm with u/c
(b) SOG0X 5.0nm with u/c
(c) DG0X 7.0nm with u/c
(d) DG0X 7.0nm with u/c

Fig. 5 The leakage current as a function of Vg decreases with increasing gate oxide thickness and applying pad-oxide undercut.

Fig. 6 The cumulative distribution of gate oxide thickness as steps of dual gate oxidation.

IGDIL (A) vs. Vd (V)

< Gox 5.0nm
> Gox 5.0nm

Fig. 8 The GIDL current of cell array as a function of Vd. The GIDL current decreases as increasing the gate oxide thickness.

Fig. 9 The refresh characteristics of cell array as a function of Fail bit count are drastically improved with increasing the gate oxide thickness.

Fig. 10 The HCI characteristics of DG0X (5.0nm) nmos are comparable enough to SOG0X (5.0nm) DRAM samples.