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Low Power CMOS Process Technologies and Characteristics for advanced High Density Mobile DRAM

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I. Introduction

A new fabrication process is required to produce high density (≥ 128M) low power DRAMs for mobile equipment. Therefore, a decrease in the gate oxide thickness in the logic area for a larger current and an increase in the gate oxide thickness in the cell array for a longer cell array refresh time is considered to be the optimum process. For this reason, a dual gate oxide (DGOX) process was adopted [1,2]. Preliminary reports show the gate oxide thinning effects of a shallow trench isolation (STI) active edge and other parameters [3,4]. In this paper, a low power DRAM (Vcc=1.8V) with a sub-0.17㎛ fabrication process and superior performance characteristics to a conventional DRAM (Vcc=3.3V) with single gate oxide (SGOX) is reported. In addition, for a mass productively stable and simple process, the optimized STI and transistor process technology was investigated. Accordingly, the STI process with the pad-oxide undercut process by wet etching before the STI gap fill process was used to release the STI top edge stress-induced leakage current [3,5]. The optical proximity correction (OPC) was used to decrease the gate CD increase according to the pattern loading effect, and the boron channel dose control was used to correct the electrical parameters (Vth, Id, BV, etc).

II. Experimental

Fig. 1 illustrates the front-end key process steps for the low power DRAM with a dual gate oxide. CMOS with SGOX and DGOX were fabricated with a 0.17 μm cell array and a minimum 0.26 μm in periphery area using a polycide gate CMOS process, having 6.5nm pure SiO_2 dry oxide in the conventional SGOX samples and 7.8nm (in the cell and high Vcc periphery) / 5.0nm (in the core and periphery) pure SiO_2 dry oxide in the DGOX ones. Boron channel implantation into the substrates at 30~40KeV through a screen oxide layer was done to optimize the transistor performance. The first gate oxides were grown in the 6.5nm pure SiO_2 dry oxide at 850℃ in the DGOX samples. However, 2.3~8.0nm pure SiO_2 dry oxide was used in the SGOX samples. In the DGOX samples, the region of thin (5.0nm) and thick (7.8nm) gate oxides was separated by added resist patterning on the wafer to expose the thin oxide region, BOE etching was used to produce the first oxide, and second pure SiO_2 dry oxide (5.0nm) was grown at 850℃. After patterning the polycide gate, a Si_xN_y spacer was formed for the lightly doped drain (LDD) and the rapid thermal annealing (RTA) at 980℃ for 10 seconds was used for the As+ activation of the nmos source/drain junction with a $3.0x10^{15}/cm^2$ dose for nmos. Finally, P+ ion implantation was done with $5.0x10^{15}/cm^2$ for the pmos. The transistor characteristics were measured with a HP4156 and the vertical structure was examined using TEM analysis. Fig. 2 shows the process flow of the dual gate oxidation and STI top edge rounding. The second oxidation could also be grown with dry oxidation because the smoothly curved active corner increased by over 10% in edge oxide thickness, which improved the productivity.

III. Results and Discussion

Fig. 3 shows a TEM image of the STI top edge profile after growing the second oxide with or without a pad-oxide undercut. The STI active corner with the pad-oxide undercut was very smooth compared to the case without. The wet etching (LAL chemical) time was in the range of 30~50 seconds and the lateral length of the pad-oxide undercut was approximately 15nm and the thickness was approximately 16nm. The curvature of the leakage current in the 32M cell array as a function of the breakdown field was similar in the sample, but the DGOX cell array decreased by approximately 1V (4.6%) compared to the other samples, as shown in Fig. 4. The curvature of the leakage current as a function of Vg was also similar between the samples and the leakage current decreased by approximately 1.3V (15%) with increasing gate oxide thickness and applying pad oxide undercut treatment, as shown in Fig. 5. This suggests that the thick oxide quality of the DGOX slightly decreases relative to that of the SGOX due to dual oxidation. However, the leakage current decreased with increasing thick oxide thickness of the DGOX. Fig. 6 shows the cumulative distribution of the gate oxide thickness as dual gate oxidation steps. The cleaning conditions before the second oxidation was only SC1 300 seconds without a HF clean causing an oxide defect failure in the thick oxide region. It is important that the remaining oxide after wet etching the first oxide in the thin oxide region must kept under 3Å due to the degradation of the thin oxide quality in the periphery. Fig. 7 shows the I-V characteristics of the nmos and pmos as a function of the gate length. The boron dose of the DGOX added should be approximately 30% for the same Vth of the SGOX with the 6.5nm gate oxide due to segregation into the Si/SiO_2 interface during gate oxidation and elimination of the first oxide with BOE etching [6]. The saturation current (Id) of the DGOX nmos and pmos increases approximately 12% at a similar Vth of the SGOX due to a decrease in the gate oxide thickness. The Vthn and Idn of DGOX nmos with the thick oxide increases and decreases approximately 40% (Vthn: 0.60V→0.85V, Idn: 1.85mA→1.20mA) compared to that of the thin oxide. Fig. 8 shows the GIDL current of the cell array with the V_{DG}. The GIDL current decreases 50% and the cell channel boron dose decreases 7% for the same cell Vth due to an increase in the gate oxide thickness (6.5nm→7.8nm, 20%↑). The refresh characteristics of the DGOX samples were improved by a decrease in the GIDL current, a decrease in the electrical field due to the decrease in the boron dose, and STI top corner stress relief. The refresh failure of the DGOX samples was generally lower than that of the SGOX due to reasons previous stated, as shown in Fig. 9. The refresh time of DGOX samples was approximately 350~400msec and improved over 15% in the DGOX samples. Fig. 10 shows that the nmos hot carrier immunity (HCI) characteristics of the DGOX sample were comparable to the SGOX due to the oxide cleaning optimization.

IV. Conclusion

The process of a wet etching for pad-oxide undercut to smooth the STI active top edge and dual gate oxidation due to an improvement in MOSFETs performance for a low power (Vcc=1.8V) DRAM was investigated. A combination of these processes greatly improved the saturation current, the leakage current, and the refresh characteristics. Therefore, the gate oxide in our DGOX process was all grown under dry oxidation, which improved the productivity. Nmos HCI characteristics of the DGOX samples were comparable to the SGOX due to the oxide cleaning optimization.

V. Reference

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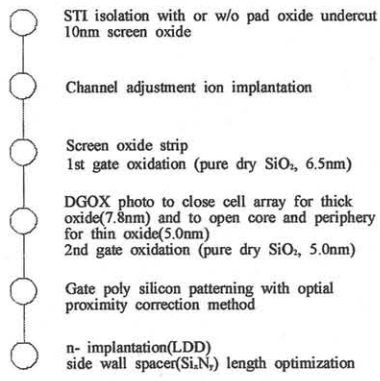

Fig. 1 The front-end key process steps for low power DRAM with dual gate oxide. The gate oxide thickness of Conventional DRAM is 6.5nm and that of low power DRAM (DGOX) is 7.8nm and 5.0nm in the thick and thin region, respectively.

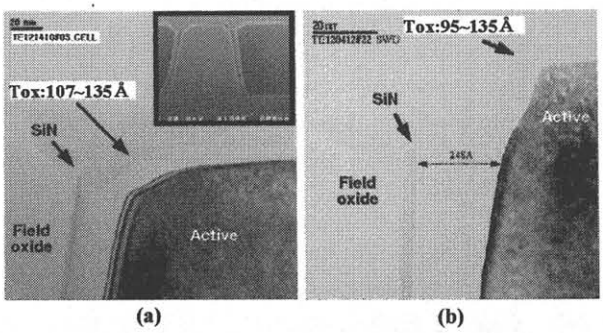

Fig. 3 TEM and VSEM images of STI top edge profile after the second oxidation. (a) STI corner round of active with wet etching for pad oxide undercut is smooth, (b) and very steep in the case without wet etchching for pad oxide undercut.

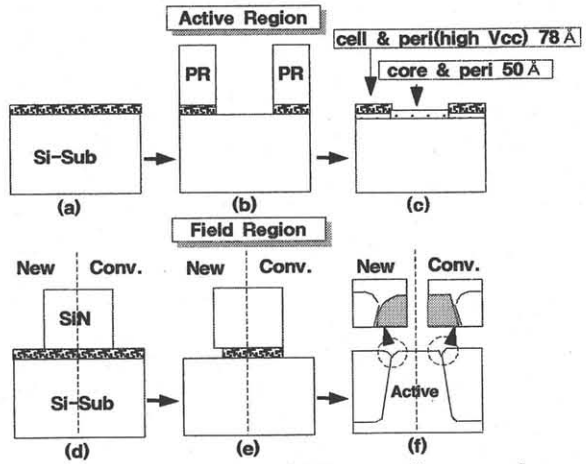

Fig. 2 The dual gate oxidation and STI top rounding process flow. (a)1st Gox 6.5nm, (b)After DGOX photo & thin oxide strip, (c)After 2nd Gox 5nm, (d)After active patterning, (e)Pad oxide wet etch undercut before STI gap filling, (f) Before gate poly-Si deposition

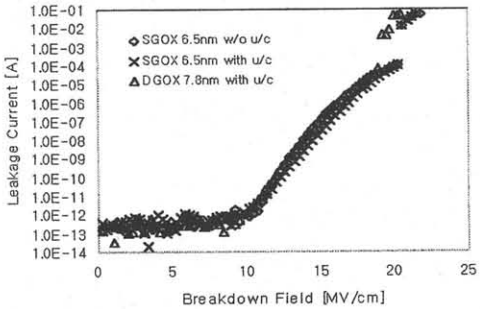

Fig. 4 The leakage current as a function of breakdown field in the 32M cell array. The curvature is similar in the sample.

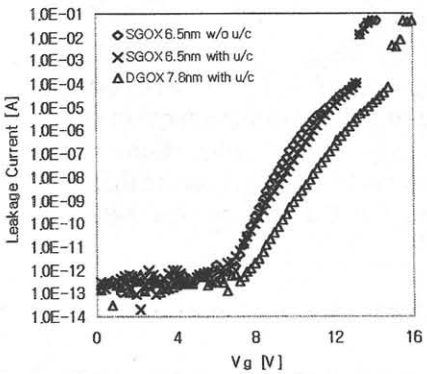

Fig. 5 The leakage current as a function of Vg decreases with increasing gate oxide thickness and applying pad-oxide undercut.

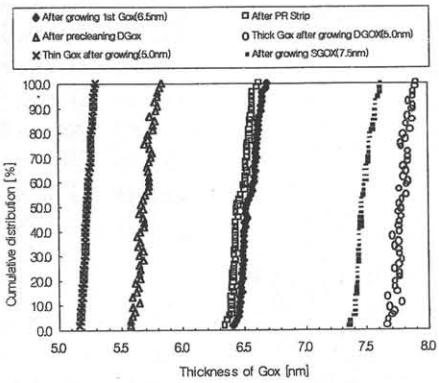

Fig. 6 The cumulative distribution of gate oxide thickness as steps of dual gate oxidation.

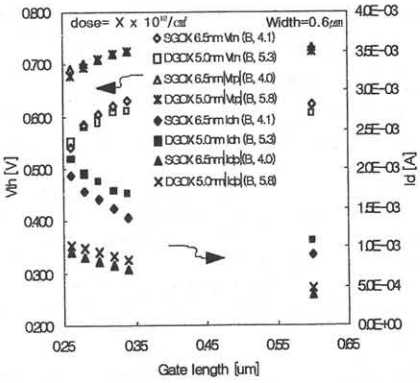

Fig. 7 The threshold voltage and suturation current of nmos and pmos as a function of gate length.

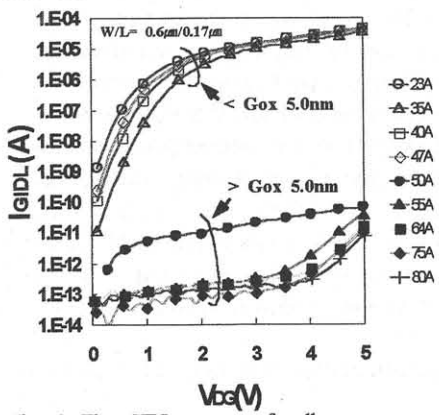

Fig. 8 The GIDL current of cell array as a function of V_{DD}. The GIDL current decreases with increasing the gate oxide thickness.

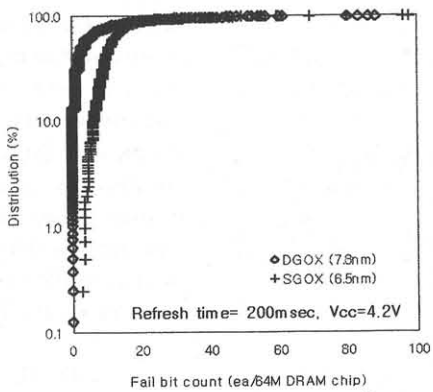

Fig. 9 The refresh characteristics of cell array as a function of Fail bit count are drastically improved with increasing the gate oxide thickness.

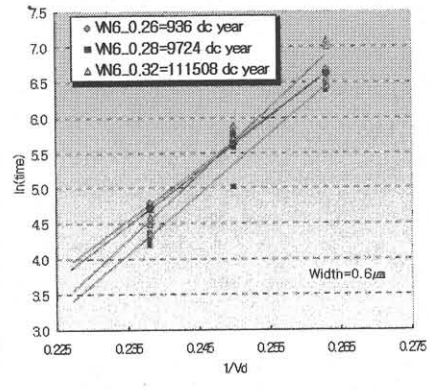

Fig. 10 The HCI characteristics of DGOX (5.0nm) nmos are comparable enough to SGOX (5.0nm) DRAM samples.