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Fabrication and electrical properties of buried tungsten structure for direct three dimensional integration

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1. Introduction

Scaling of integrated circuits has improved to meet circuit performance and feature size for the last several decades. Three dimensional (3-D) integration has been considered as one of the most promising candidates because of its higher integration density and lower interconnection complexity and delay. According to Zhang et al. [1], nearly 40 % area reduction with 18 % interconnection delay could gain for two device layer structure while 70 % area reduction with 40 % interconnection delay could gain for four device layer structure. In addition, 20 %-25 % reduction in power dissipation has also been reported [2].

For implementation of 3-D integration, in the past, several different approaches, such as selective lateral overgrowth, laser recrystallization and metal-induced lateral crystallization, have been explored [3, 4]. The selective lateral overgrowth, however, requires high temperature and time, leading to limitations on the design of transistor and its connectors. On the other hand, the recrystallized silicon using either lasers or other energy providing techniques has limitations to form well grain boundary.

To overcome such limitations, our group has introduced and developed a low temperature approach to single crystal silicon layering to obtain multi-layers with buried structures for fabricating direct 3-D integrated circuits [5]. Here the single crystal layering was implemented at the temperature as low as 450 °C. It is comparable to some of the steps in back-end-of-line processing of CMOS, thus removing a significant constraint in the practice of three-dimensional integration. At the above work, we have fabricated and characterized of polycrystalline Si with buried structure.

Now, in this work, we have explored the tungsten with buried structures for the implementation of direct 3-D integration. Tungsten is one of the most promising candidates for metal gate and interconnection CMOS technology due to its unique properties of low resistivity compared to polycrystalline Si and high resistance to electromigration compared to aluminum. In this paper, we demonstrated the fabrication process of the buried tungsten structure and measured electrical properties - the resistivity of the buried tungsten and capacitance between tungsten fingers and layering Si.

2. Fabrication of buried tungsten structure

Low temperature oxide (LTO) was deposited in thickness of 600 nm on 4 inch p-type Si (100) at 450 °C. After that, tungsten films were deposited over patterned LTO with trench lines, which are 200 nm-deep. Here, tungsten films were deposited by tungsten CVD from tungsten hexacarbonyl [$W(CO)_6$] with ultra high vacuum system below 10^{-8} torr at 570 °C and 10 mTorr. Chemical mechanical polishing (CMP) was used for the tungsten damascene process employed to remove the surface tungsten, leaving behind tungsten filled trench. Although the roughness of both LTO and tungsten in the trench was below 0.4 nm from AFM (Atomic Force Microscopy), 20 nm deep dishing appeared at the tungsten filled trench after CMP. This kind of dishing suffers layering Si. So, for removal dishing, additional oxide were deposited by PECVD and LTO with total thickness of 600 nm on the tungsten filled trench wafer and one more CMP process carried out.

Smart-cut process [6] was carried out for layering Si. The layering Si wafer, called donor wafer, was implanted with hydrogen ions (H^+) at 100 KeV with $3x10^{16}$ cm^{-2} through 10-nm oxide. The thickness of layering Si was 700 nm. Before direct wafer bonging, both tungsten filled trench wafer and donor wafer were cleaned in a modified RCA cleaning. This step results in hydrophilic clean oxide surfaces. After direct bonding, we performed very low temperature annealing to improve bonding strength and the splitting temperature was 450 °C. Figure 1 shows surface of buried tungsten trench wafer after layering Si. The yellow region is layering Si area and 70 % areas are covered.

The LOCOS process at 1000 °C was performed for making active area in the layering Si. The tungsten finger

pattern is located below active area on the layering Si in Fig 2. For examination of electrical properties buried tungsten structures, we made capacitors and resistors.

3. Electrical properties of buried tungsten layer

We got the tungsten film with a resistivity of 18 μΩ-cm after deposition. Sheet resistance and resistivity of tungsten lines were measured and calculated with variable length and width from I-V plot. The sheet resistance was around 13 Ω/sq. The resistivity after all the processes was up to around 200 μΩ-cm. The capacitance of oxide between tungsten fingers and active area of layering Si were measured at 100 kHz in Fig. 3.

4. Conclusion

We have explored buried tungsten structure that is made of layering Si for the implementation of direct 3-D integration. The layering Si process, called smart-cut, is based on hydrogen implantation and wafer bonding. Thin silicon layer can split and transfer the main wafer at low temperature (450 °C). Our tungsten films were deposited by using of tungsten hexacabonly ($W(CO)_6$) in ultra high vacuum system (10^{-8} torr) at 570 °C and 10 mTorr. For embodiment of buried tungsten structure, we patterned LTO deposited on 4 inch Si (100) wafer. Tungsten films were deposited on trench patterned LTO wafer followed by chemical-mechanical polishing. Smart-cut process was then performed. Silicon wafers for layering were n-type Si (100) and implanted by H^+ with $3x10^{16}$ ion/cm^2 at 100 KeV. We made resistor and capacitor for charactering electrical properties and measured electrical properties - the resistivity of the buried tungsten and capacitance between tungsten fingers and layering Si.

Acknowledgement

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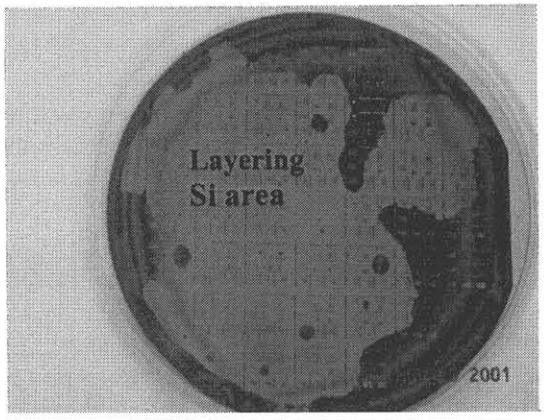

Fig. 1 . Optical micrograph of the surface after layering Si.

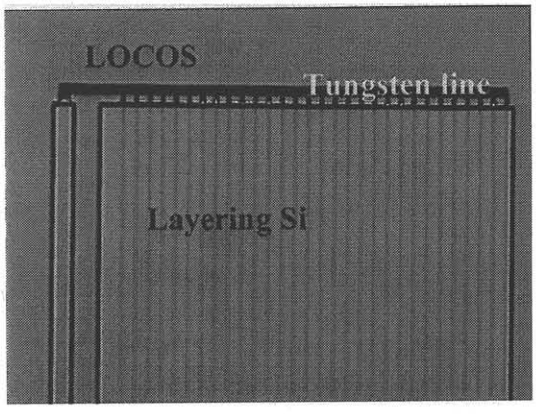

Fig. 2 Optical micrograph of the surface after formation of active area on the layering Si.

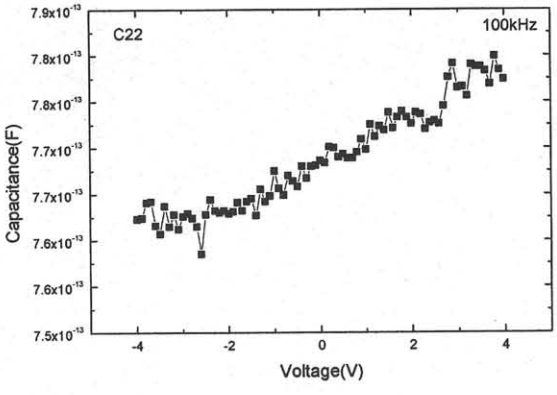

Fig. 3 C-V plot got from tungsten fingers and active area on the layering Si.