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Novel Nanoprocess for Vertical Double-Gate MOSFET Fabrication by Ion-Bombardment-Retarded Etching

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1. Introduction

A double-gate (DG) MOSFET has been regarded as one of the most promising candidates beyond bulk CMOS devices due to its inherent robustness to short-channel-effects (SCEs) and improved current drive capability[1,2]. Especially a vertical DG MOSFET is very attractive because of its process compatibility with standard CMOS devices and its suitability with bulk Si substrates[3,4]. The critical issue is a fabrication technology for an ultrathin Si wall of the DG MOSFET enough to guarantee high performance. The fabrication of vertical ultrathin Si walls on a bulk Si substrate with a conventional RIE process is rather difficult as depicted in Fig. 1. Si wall thinning by over-etching technique is impossible because of a lack of an etch-stopper in the bulk Si. Also the etched corner at the bottom of the Si wall becomes round. Moreover serious damage by the RIE process is introduced into the Si wall.

In this work, we have found the retarded etch rate (ER) of ion-beam-exposed Si in the tetramethylammonium hydroxide (TMAH) solution. This paper describes that the newly found phenomenon, i.e., the ion-bombardment-retarded etching (IBRE), makes it possible to easily fabricate an ultrathin Si wall for the vertical DG MOSFET on a bulk Si substrate without any RIE process damage.

2. Experimental

We used a p-type Si(110) wafer with a 70-nm-thick SiO_2 layer as a mask. The SiO_2 mask was patterned by using an EB lithography and an RIE process. Both forming and thinning of the Si wall were performed by dipping in the 2.38% TMAH solution at 50°C, which is well-known as a resist developer and also as an isotropic etchant. The ERs of (110)- and (111)-oriented Si in the TMAH at 50°C are 260 and 20 nm/min, respectively. To investigate the IBRE, Arsenic ions at 30 keV were implanted onto the Si substrate with the dose of 3×10^{12}-10^{15} cm^{-2}.

3. Results and Discussion

The dose dependence of the ER of Si(110) substrate in the TMAH solution has been investigated and the results are shown in Fig. 2. The ER of Si is markedly decreased at a dose over 3×10^{13} cm^{-2}. This phenomenon arises from the suppression of electrochemical reaction between the Si substrate and the TMAH due to the increase in the resistivity of Si as a result of ion bombardment. Thus, the Si region exposed to 30 keV As ions with a dose over 3×10^{13} cm^{-2} can work as an etch-stopper against the TMAH solution.

The process flow for the ultrathin Si wall fabrication by using the newly found IBRE is outlined in Fig. 3. The cross-sectional SEM pictures for each step are shown in Fig. 4. First, the SiO_2 mask with a line-pattern parallel to the <112> direction was formed on a Si(110) substrate. Then the Si substrate was anisotropically etched with TMAH for 25 sec to form the 55-nm thick Si wall with a height of 100 nm (Fig.4(a)). The perpendicular side wall is (111)-oriented. Second, the SiO_2 mask was completely stripped away and 30 keV As ions at a dose of 1×10^{15} cm^{-2} were irradiated perpendicularly to the Si surface using a conventional ion implanter (Fig. 4(b)). As a result, the top and bottoms of the Si wall were exposed to keV ions, while the sidewalls remained virgin. Finally, the sample was again dipped in TMAH for 1 min. Then the ion-exposed-regions (top and bottom) effectively served as an etch-stopper and the Si wall was horizontally etched. The ER of (111)-oriented sidewall is extremely low, ensuring a very good control of the Si wall thinning. Consequently, a 16-nm thick ultrathin Si wall was successfully formed as shown in Fig. 4(c). The ion-exposed regions, i.e., the top and bottoms of the Si wall, turn to the drain and source of the DG-MOSFET. Thus, our processes have the great advantage of no damage introduction due to both the RIE process and the ion implantation into the Si sidewall.

We explored the effectiveness of Si wall thickness for the vertical DG MOSFET performance by using process/device simulations. First, we modeled the vertical DG MOSFET followed by the developed processes using a process simulation[5]. The process flow and parameters which we used are summarized in Fig. 5(a). The effective channel length was estimated to be 25 nm according to the simulated As profile as shown in Fig. 5(b). Using the obtained structures, the device simulation[6] was performed. The simulated influence of the Si wall thickness on the subthreshold slope (S-slope) is shown in Fig. 6. It can be concluded that, for 25 nm channel length vertical DG MOSFET, the Si wall thickness below 30 nm is demanded for the suppression of the SCE.

4. Summary

A novel Si nanoprocess has been developed using the newly found ion-bombardment-retarded etching (IBRE) phenomenon of Si in the tetramethylammonium hydroxide (TMAH) solution. Using the process, we have succeeded in fabricating the vertical ultrathin Si wall with 16 nm thickness on the bulk Si substrate without any dry etching damage. The simulation results show that, for 25 nm channel length vertical DG MOSFET, the Si wall with 16 nm thickness is satisfactory for the suppression of the SCE.

Acknowledgements

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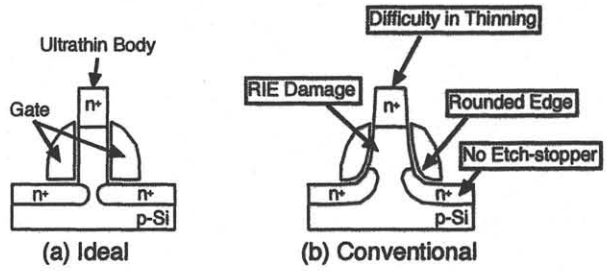

Fig. 1 Comparison between (a) ideal vertical DG MOSFET and (b)actual one fabricated with an conventional RIE process.

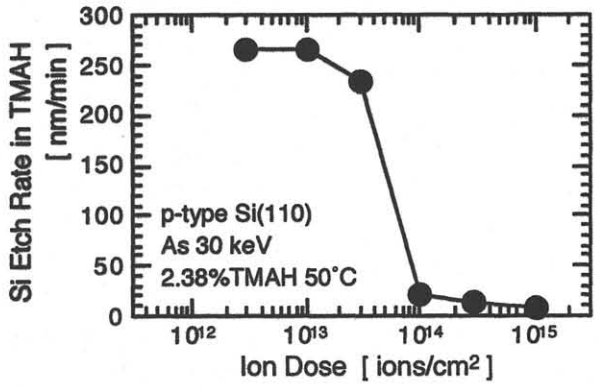

Fig. 2 Dependence of etch rate of Si in TMAH on 30 keV As ion dose.

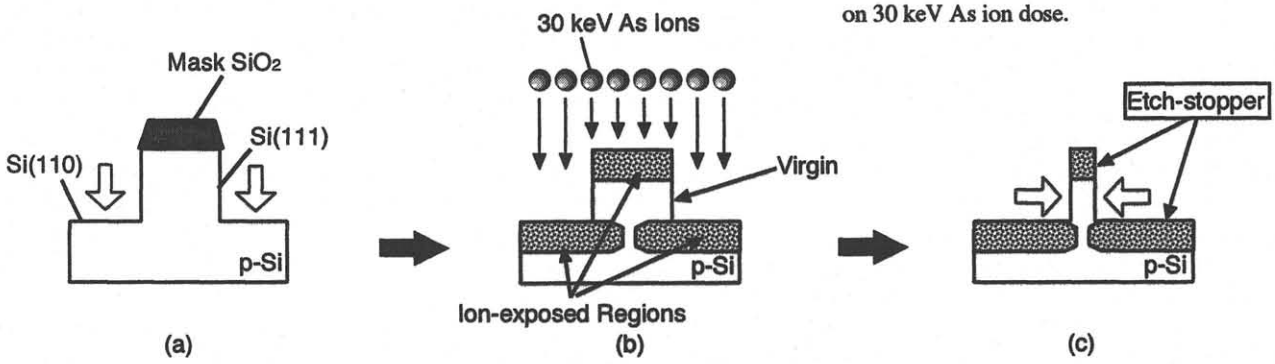

Fig. 3 Ultrathin Si wall fabrication process flow: (a) thicker Si wall formation by vertical etching using an SiO_2 mask, (b) mask SiO_2 stripping and ion implantation, and (c) ultrathin Si wall formation by using IBRE.

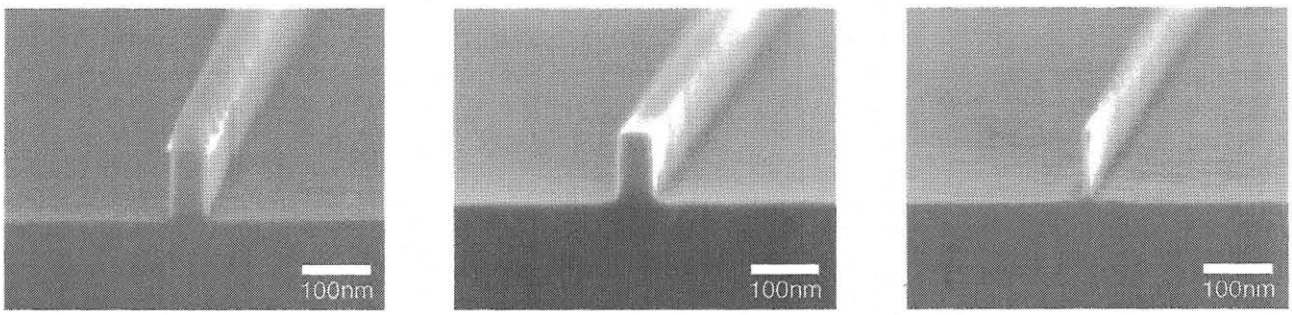

Fig. 4 Cross-sectional SEM images of Si walls for each step: (a) after the vertical etching using an SiO_2 mask, (b) after the SiO_2 mask stripping and ion implantation, and (c) after the thinning by using IBRE.

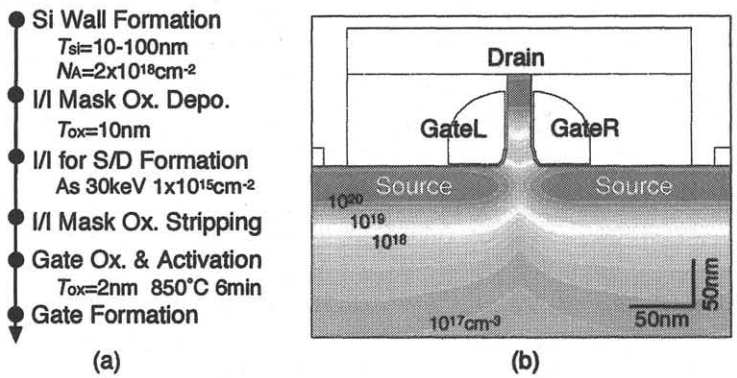

Fig. 5 (a) Process flow and parameters used in the simulation, (b) simulated device structure and As profile in the 20nm Si wall vertical DG MOSFET.

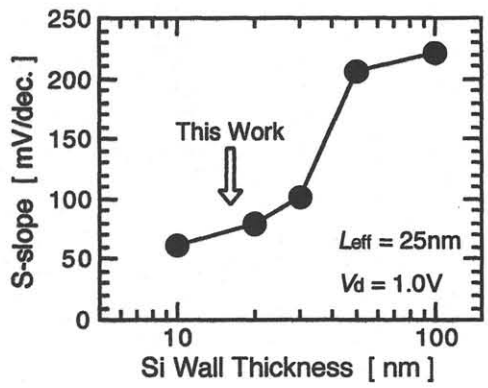

Fig. 6 The effect of the Si wall thickness on the subthreshold slope.