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Interface Defects Responsible for the Negative-Bias Temperature Instability of the Plasma-Nitrided SiON/Si Diodes

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1. Introduction

We investigated the mechanism of the negative-bias temperature instability (NBTI) of plasma-nitrided SiON/Si diodes with equivalent oxide thicknesses (EOTs) of 1.6 to 1.8 nm, by carrying out D_2 passivation annealing, conductance-frequency ($G(\omega)$) measurements and electron spin resonance (ESR) measurements. The results presented here show that the differences between the SiON/Si and SiO_2/Si diodes in NBTI lie in the nature of interfacial Si dangling bonds.

Nitrogen is introduced into the gate oxide of metal-oxide-silicon (MOS) field-effect transistors (FETs) to suppress the boron penetration from the gate poly-Si of p-MOSFETs. Additionally, N can be added by plasma nitridation [1] to lower the gate leakage current, which is evaluated with the EOT. However, the addition of N causes the critical reliability problem of NBTI [2]. For the NBTI of the SiO_2/Si system, Poindexter *et al* proposed a reaction model [3],

$$\equiv\text{Si-H} + \text{A} + \text{h}^+ \rightarrow \equiv\text{Si}\cdot + \text{A-H}^+, \qquad (1)$$

where H is transferred from the H-terminated Si dangling bond ($\equiv$Si-H) to something ancillary (A) with a hole (h^+), thus leaving a Si dangling bond (P_b center, $\equiv$Si $\cdot$) at the interface. By using resonant nuclear reaction analysis, we observed a change in the hydrogen distribution in 25-nm-thick SiO_2 upon negative-bias temperature stress (NBTS) [4]. This observation also suggests that the transport of hydrogen is involved in NBTI. However, it has not yet been confirmed whether the interfacial reaction (1) also occurs in the thin-SiON/Si MOSFETs currently being developed. Furthermore, it is not clear how the N introduction influences on the NBTI.

To check the model's applicability, we compared the NBTI of H_2-annealed and D_2-annealed diodes. Although it has already been reported that the NBTI of a MOSFET with a 3.8-nm thick SiO_2 gate is suppressed by the D_2 annealing [2], D_2's effect was not confirmed for thinner SiON gate. To characterize the NBTS-induced defects, we measured $G(\omega)$ characteristics and ESR. Such defects characterization does not seem to have been carried out on NBTS-applied ultra-thin SiON gate. Further, we performed post-oxidation annealing (POA) on our SiON gate to reduce the interface state density (D_{it}).

2. Experimental Procedures

Local-oxidation-of-Si (LOCOS)-isolated p^+ poly-Si/SiON/p(100)Si diodes were prepared. After forming the LOCOS structures, rapid thermal oxidation (RTO) and plasma nitridation were performed. The N content evaluated by X-ray photo-emission spectroscopy was 9%. After forming the B-doped poly-Si electrodes, the samples were annealed in a H_2 or D_2 ambient to passivate the interface states. The EOT of the SiON was 1.6 to 1.8 nm.

To assess the NBTI, a bias voltage of -2.8 V was applied to 0.01-mm^2 diodes at 150°C in air. After cooling the samples to RT, capacitance-voltage (C-V) and $G(\omega)$ measurements were carried out to evaluate the C-V shift (ΔV_{FB}) and the D_{it}. The $G(\omega)$ curves were corrected by taking into account the gate leakage current and series resistance.

For the defect characterization, a bias of -2 V was applied to H_2-annealed 4×8 mm^2 diodes at 150°C for 180 min. A voltage drop along these large-area gate electrodes was avoided by depositing Al on the poly-Si. After the NBTS application, the Al and poly-Si layers were removed by wet etching. The X-band (9.43 GHz) ESR was measured at 10 K. The microwave power was set at 1 mW, ac magnetic field at 1 G, and its modulation frequency at 100 kHz. For references, we measured the ESR of diodes that were annealed at 740°C in N_2 to depassivate the defects [5].

Also, we measured the D_{it} of the diodes that received POA, after annealing at 740°C in N_2. The temperature of POA was above 1000°C.

3. Results and Discussion

Effects of D_2 annealing on NBTI

In Fig. 1, ΔV_{FB} and ΔD_{it} are plotted against stress duration. The ΔD_{it} values are those estimated in the $G(\omega)$ peak frequency range of 10-100 kHz. The probed surface Fermi level (E_{FS}) is 0.3 to 0.4 eV above the valence band maximum (VBM), which corresponds to the (+/0) transition energy of the P_b centers. We confirmed that ΔV_{FB} and ΔD_{it} are negligible when the stress voltage is set at zero (ZBTS). The NBTS-induced ΔV_{FB} and ΔD_{it} of D_2-annealed diodes are lower than that of H_2-annealed diodes. This ΔD_{it} difference between the two kinds of anneal ambient suggests that the P_b-center depassivation is involved in the NBTI process of our plasma-nitrided SiON/Si diodes.

Defects induced by NBTS

P_b centers (P_{b0} and P_{b1}) were detected by the ESR

measurements of the NBTS-applied samples (Fig. 2). Comparison of the P_b spin density (3.4×10^{11} cm^{-2}) with the ΔD_{it} (4.6×10^{11} $cm^{-2}eV^{-1}$) indicates that the P_b centers are the dominant interface states caused by the NBTS. In contrast, ZBTS did not cause P_b signals. Figure 2 also shows the P_b signals of the SiON/Si and RTO/Si diodes that were annealed in N_2 for P_b depassivation. When compared with the RTO, both of the NBTS-applied and thermally-depassivated SiON diodes exhibit smaller P_{b0}/P_{b1} ratios and larger P_{b1} signal widths (SiO_2: 2.5 G, SiON: 3.6 G). These common features support the model that H is removed from the initially H-terminated P_b center upon NBTS application. The broadening of the P_{b1} signal indicates a higher strain [6] at the plasma-nitrided SiON/Si interface than that at the SiO_2/Si interface. On the other hand, defects in the SiON bulk were not detected in the NBTS-applied diodes.

Effects of POA on D_{it} of plasma-nitrided SiON/Si diodes

Figure 3 shows the D_{it} after the N_2 annealing. The D_{it} of RTO/Si without POA is not shown, since its determination was not possible due to the high leakage current. In Fig. 3, the D_{it} of plasma-nitrided SiON/Si diode is reduced by the POA. This suggests that the density of P_b centers, which are terminated by hydrogen before the thermal depassivation or NBTS application, is lowered. We attribute this effect to the P_b center reduction. This method seems promising for the suppression of NBTI, although the D_{it} is still higher than that of the RTO/Si diodes which received POA.

4. Conclusion

The NBTI of plasma-nitrided SiON/Si diodes with EOTs of 1.6 to 1.8 nm was shown to occur through P_b depassivation. The increase of P_b center density and strain around the P_b centers is thought to be a cause of the higher NBTI of the SiON gate.

References

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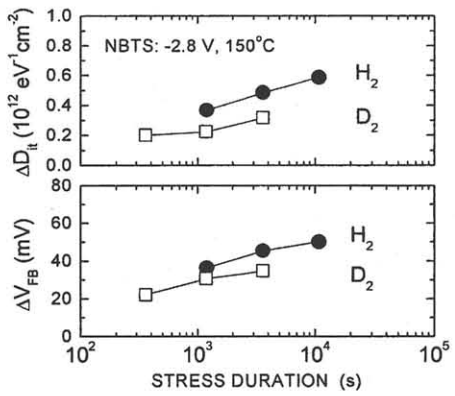

Fig. 1 C-V shift (ΔV_{FB}) and increase of interface state density (ΔD_{it}) of H_2- and D_2-annealed plasma-nitrided SiON/Si diodes plotted against duration of NBTS. The bias voltage and temperature of NBTS are -2.8 V and 150°C, respectively. The ΔD_{it} values are those at the surface Fermi level 0.3 to 0.4 eV above the valence band maximum.

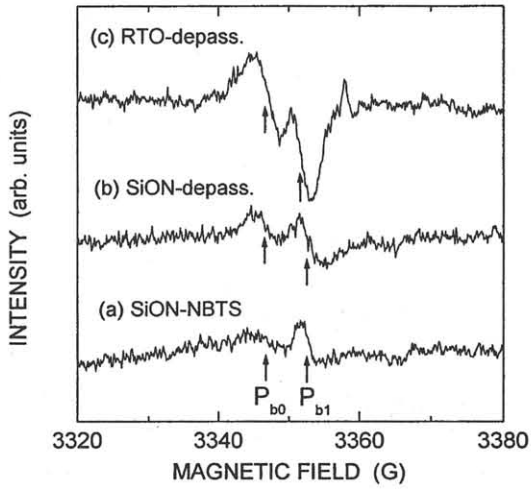

Fig. 2 ESR signals of the P_b centers detected for (a) the NBTS-applied SiON/Si, (b) thermally depassivated SiON/Si, and (c) thermally depassivated RTO/Si diodes. The magnetic field is set parallel to the [100] axis.

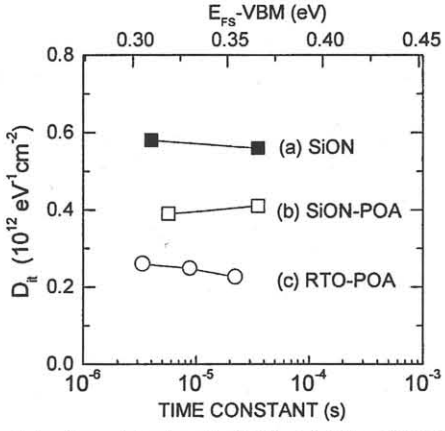

Fig. 3 Interface state density (D_{it}) of (a) the SiON/Si diode, (b) SiON/Si diode subjected to POA, and (c) RTO-Si diode subjected to POA. The D_{it} values are plotted against the peak frequency of the $G(\omega)$ curve measured at RT. The corresponding surface Fermi level is calculated assuming a hole capture cross section of 10^{-16} cm^2. All the diodes were annealed in N_2 at 740°C before the $G(\omega)$ measurements for P_b depassivation.