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Integrity of Gate Oxide grown on Si implanted Si-substrate

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ABSTRACT

We studied the characteristics of gate oxide grown on Ge or Si implanted Si substrates (Ge I/I oxide and Si I/I oxide), of which the implantation enhances the oxidation rate. Si implantation produces less enhancement in oxidation rate compared to that of Ge implant case but yields electrical characteristics comparable to control SiO_2. Although the Q_{bd} of Si I/I oxide with 1E15cm^{-2} grown at 750°C was observed to be degraded, it can be improved under high oxidation temperature of 800°C. This improvement is attribute to the reduced charge trapping and improved interface characteristics as manifested by the reduced hysteresis and interface state density (D_{it}).

INTRODUCTION

System-on-a-chip having multiple supply voltage has gradually drawn attraction for the requirement of various device products. One of the approaches for satisfying the requirement is the application of multiple gate oxide on a chip. A simple technique to realize the multiple gate oxide is the use of implantation method to modify oxidation rate. Oxide grown on N implanted Si-substrate (N I/I oxide) was shown to reduce oxide growth rate; however, N I/I oxide showed the high oxide trap density (N_{ot}) and poor reliability characteristics[1,2].

In this paper, we investigated the enhanced oxidation process using Ge and Si implant for multiple gate oxide, and characterized the gate oxide integrity (GOI) of Ge I/I oxide and Si I/I oxide. Ge and Si were chosen in order to avoid the chemical effects due to implanted elements on the GOI.

EXPERIMENTAL

n+Poly-Si/ SiO_2/Si nMOS capacitors with shallow trench isolation (STI) were fabricated on the p-type (100) Si sub.(8-inch dia.). After a photoresist patterning, Ge or Si were implanted at the energy of 7keV with the doses ranging from 1E14 to 1E15cm^{-2} on the screen oxide (50 Å) and followed by the photoresist and screen oxide strip. Gate oxidation was then carried out in a conventional furnace under H_2O ambient at 750°C or 800°C to grow gate oxide having different thicknesses.

RESULTS AND DISCUSSION

Shown in Fig.1 is the growth behavior of Ge I/I oxide. With increasing Ge doses, the oxide thickness increases for the same oxidation time. Fig.2 exhibits J-V curves of nMOS capacitors having Ge I/I oxide with the Ge dose of 3E14cm^{-2}. It is noted that the leakage current of Ge I/I oxide at low electric filed is about 5 orders of magnitude higher than that of control SiO_2. The reason for this observation is not clear, but it could be related to the Ge pile-up on the SiO_2/Si interface[3]. The large interface states (high-10^{10} /cm^2-eV) shown in Fig.3 also should be attributed to the phenomena.

Figure 4 plots the growth characteristics of Si I/I oxide grown in H_2O ambient at the temperature of 750°C. It is clear that the oxidation enhancement is not as effective as Ge implant case, at best 8~9 Å difference. This is because oxidation enhancement due to Si implant mainly depends on the amount of implant damage. The saturation behavior of oxidation enhancement over 3E14cm^{-2} doses, which is a critical dose for amorphization, supports this argument. Fig.5 exhibits the XTEM images. The rough Si surface after Si implant was observed to recover during gate oxidation. Fig.6 shows C-V curves of Si I/I oxide with Si doses for the same oxidation time. The capacitance equivalent thickness (CET) increases with increasing Si doses, but all of the C-V curves show no flatband voltage (V_{fb}) shift as compared to control SiO_2, suggesting negligible oxide charge in oxide generated by Si implant. Although the oxidation rate of Si I/I oxide is lower than that of Ge I/I oxide, Si I/I oxide exhibits leakage current comparable to that of control SiO_2 as shown in Fig.7. Fig.8 exhibits Q_{bd} characteristics with Si doses. There was no Q_{bd} degradation for Si doses below 5E14cm^{-2}, whereas the Si I/I oxide with 1E15cm^{-2} dose was found to exhibit the reduced Q_{bd}. We also overlapped the reliability characteristics of Si I/I oxide with 1E15cm^{-2} grown at the oxidation temperature of 800°C. It should be noted that the Q_{bd} of 800°C samples was similar to that of control SiO_2.

In order to understand the reason of the reliability improvement of the Si I/I oxide grown at 800°C, we probed the characteristics of hysteresis before and after constant current stress as shown in Fig.9. Although there was no hysteresis for all of the fresh samples, hysteresis appeared after electrical stress. The C-V curves also show the negative shift of the V_{fb} and the non-ideal hump region, indicating that abnormal positive charges and interface states were generated within the oxide and SiO_2/Si interface during stress, respectively. Fig. 10 exhibits the N_{ot} with Si doses, which can be calculated from the area of the hysteresis[4]. It was found that the higher the Si dose is, the higher becomes the trap density. The N_{ot} of Si I/I oxide having 1E15cm^{-2} grown at 800°C, however, was lower than that of 750°C samples. This result suggests the reduced charge trapping under stress and improved reliability of 800°C samples. Fig.11 exhibits the conductance loss (G/ω)-log ω plots of MOS capacitors for interface state density (D_{it}) extraction. The D_{it} level was approximately in the medium-10^{10} /cm^2-eV for all samples, whereas the SiO_2 I/I oxide with 1E15cm^{-2} grown at 750°C has higher conductance loss at the given voltages ranging -0.76 to -0.82V, which corresponds to the flatband edge to the midgap of Si. It indicates that the interface states were generated across the Si or SiO_2 bandgap by the high dose Si implant. The samples grown at 800°C, however, were observed to have lower D_{it} at the same voltages. It is known that a Si dangling bond, i.e., trivalent Si atom, introduces a deep trap level near the Si midgap and in the SiO_2 bandgap[5]. Therefore, it can be inferred that some of the excess Si existing in oxide by Si implant probably roles as the defects at the SiO_2/Si interface and/or in the oxide, resulting in the degradation of the reliability. It was also reported that the SiO_2/Si interface characteristics depend on the oxidation temperature; the D_{it} is improved by increasing oxidation temperature[6]. This suggests that the higher oxidation temperature improves the D_{it} of Si I/I oxide and enables Si I/I oxide to have immunity under the high electrical stress, resulting in the reliability improvement as confirmed by the suppressed D_{it} and the N_{ot} under electrical stress.

CONCLUSION

We studied the characteristics of MOS capacitor with Ge I/I oxide and Si I/I oxide. Ge I/I oxide shows large leakage current and D_{it}, whereas Si I/I oxide with below 5E14cm^{-2} has characteristics comparable to control SiO_2. The Q_{bd} of Si I/I oxide with 1E15cm^{-2} grown at 750°C was observed to be degraded; however, it can be improved under high oxidation temperature of 800°C. Although the thickness increase using Si implant is small, this technique is applicable for multiple gate oxide processes because of good electrical quality.

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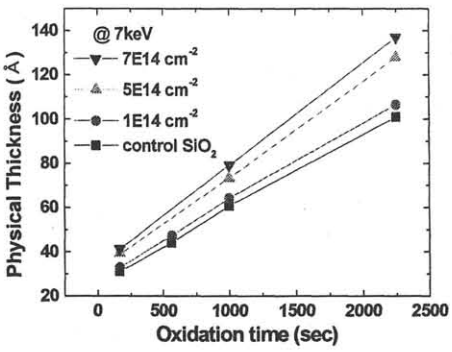

Fig. 1. Physical thickness of Ge I/I oxide vs. oxidation time with Ge implant doses.

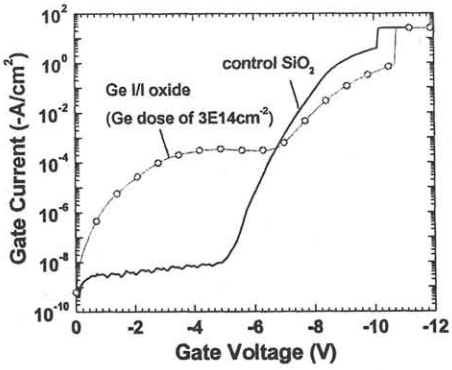

Fig. 2. J-V plots of nMOS capacitors with control SiO_2 and Ge I/I oxide.

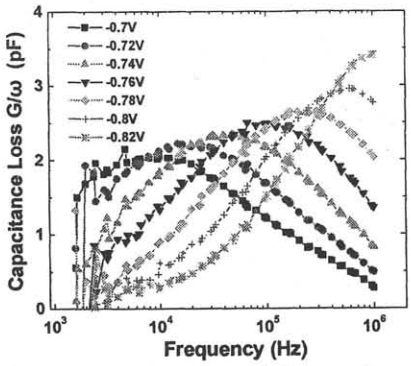

Fig. 3. Conductance loss (G/ω) -log ω plots of Ge I/I oxide with the dose of 3E14cm^{-2}.

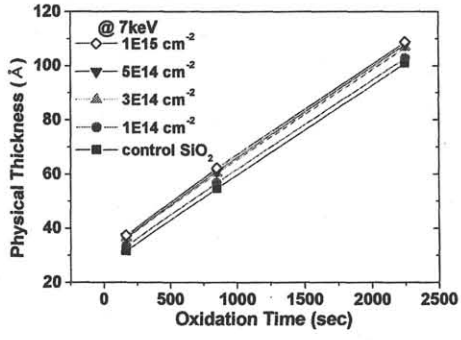

Fig. 4. Physical thickness of Si I/I oxide vs. oxidation time with Si implant doses.

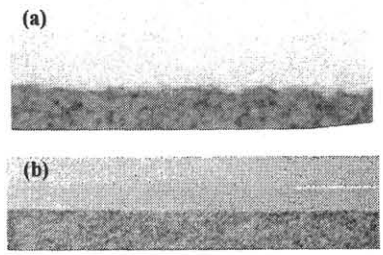

Fig. 5. XTEM image (a) after Si implant on sacrificial oxide, (b) after gate oxidation.

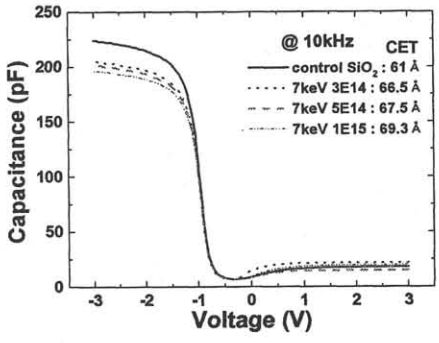

Fig. 6. C-V characteristics of nMOS capacitors having Si I/I oxides grown during the same oxidation time.

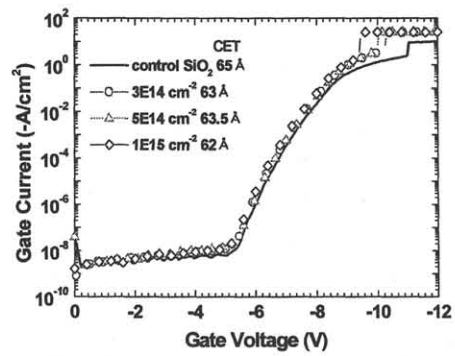

Fig.7. J-V curves with nMOS capacitors having the similar CET as a function of Si implant doses.

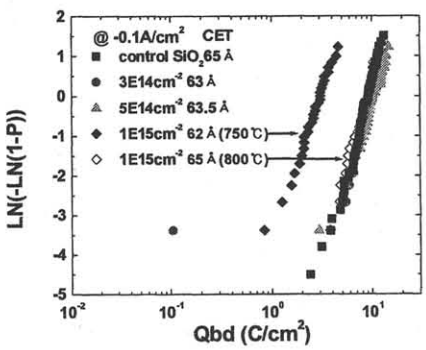

Fig. 8. Qbd characteristics with Si implant doses.

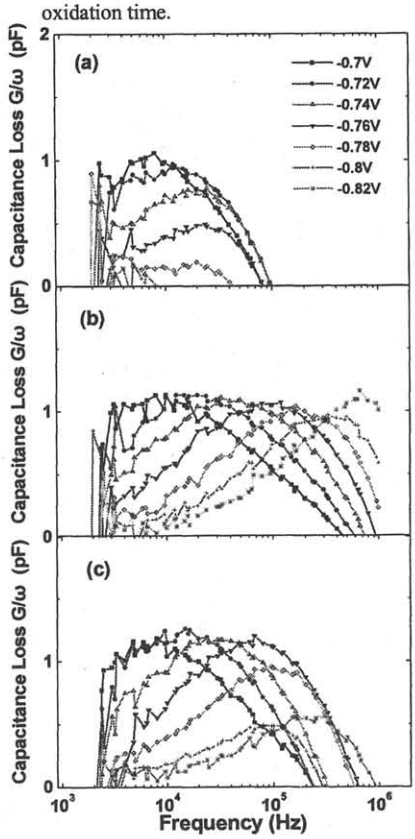

Fig. 11. Conductance loss (G/ω) -log ω plots, (a) control SiO_2, Si I/I oxide with 1E15 cm^{-2} grown at (b) 750℃,and (c) 800℃

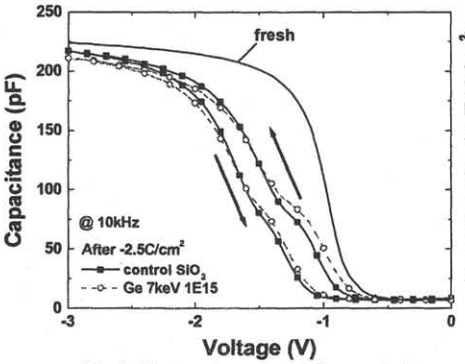

Fig.9. Hysteresis curves before and after -2.5C/cm² stress.

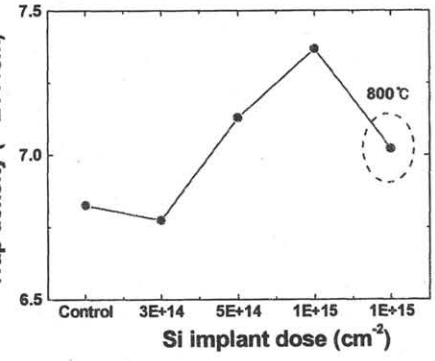

Fig.10. Oxide trap density after -2.5C/cm².