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Novel Nickel Silicide Formation Technique for Sub-50nm MOS Device Application

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1. Introduction

With the aggressive scaling-down of CMOS devices, the parasitic resistance associated with the source/ drain junction becomes one of the major concerns for improving device performance, and hence the lower resistive silicide has been aggressively investigated. [1] Nickel silicide is one of the promising candidates for future silicide, because it has the low resistivity, low contact resistance and no line width dependence. However, there are difficulties in sustaining its low resistance at higher temperature for composite nickel silicide especially when the thickness of deposited and composed nickel is thin. [2]

In this paper, we proposed multi-step annealing method as a new nickel silicide formation technique which is suitable for sub 50nm MOSFET. This paper represents the experimental methods and results for the nickel silicidation on bulk Si wafers.

2. Experiments and Results

An annealing with single temperature rising period (50°C/sec and 200°C/sec) and holding period (30sec each) has been applied to 40nm thick nickel film deposited on bulk Si wafers [2][3]. In this method, the annealing temperature to sustain a low resistance could not be increased over 400°C, because agglomeration of Ni occurred on the surface as shown in Fig.1.

In order to solve this problem, we propose a new nickel silicide formation technique called as "multi-step annealing method" which has the temperature holding times of 30sec at every 50°C in increasing the temperature rising period as shown in Fig.2 (a). A nickel silicide with lower resistance, which can sustain its low resistance up to 600°C, could be obtained by the multi-step annealing method as shown in Fig.2 (c). Furthermore, we could obtain a nickel silicide with lower resistance and sustain its low resistance up to 800°C by increasing the temperature holding time at maximum temperature as shown in Fig.2(b) and (d). Figure 3 shows SEM micrographs of the nickel silicide surface. The clean surface without agglomeration could be obtained up to 800°C.

To certify the effects of temperature holding steps, we examined the normal annealing method with the monotonous increase of annealing temperature which has the identical rising and holding times of annealing temperature with those of multi-step annealing method as shown in Figs. 4 (a) and 4 (b). The sample of multi-step annealing gave mirror like clean surface as shown in Fig. 4 (c), while normal annealing showed agglomeration on the surface as shown in Fig. 4(d). Resulted sheet resistance of nickel silicide formed from 20nm thick nickel deposited on bulk Si wafer is shown in Fig. 5. Comparing to normal annealing, lower resistance could be achieved at higher temperature in the multi-step annealing method.

Next, the post annealing effects were evaluated as shown in Fig.7. After multi-step annealing to form nickel silicide, the post annealing was carried out to evaluate thermal stability of nickel silicide. As shown in this figure, the resistance did not show any changes up to 700°C. Therefore, we concluded that nickel silicide formed by the multi-step annealing method has excellent thermal stability.

3. Conclusions

We proposed the multi-step annealing method as a new nickel silicide formation technique with high thermal stability. It is suitable for sub 50nm MOSFET. By using this multi-step annealing method, low sheet resistance stable up to higher temperature could be achieved without agglomeration and even when the deposited nickel thickness was as thinner as 20nm, low sheet resistance could be sustained up to 800°C.

References

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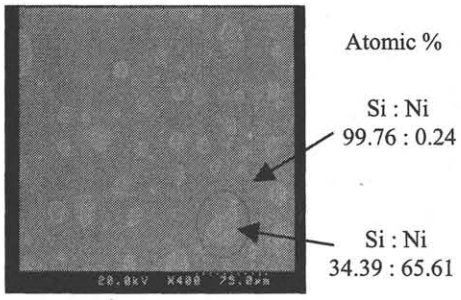

Fig. 1 SEM and EDX result of nickel silicide sample annealed at 500°C with 200 °C/sec temperature gradient.

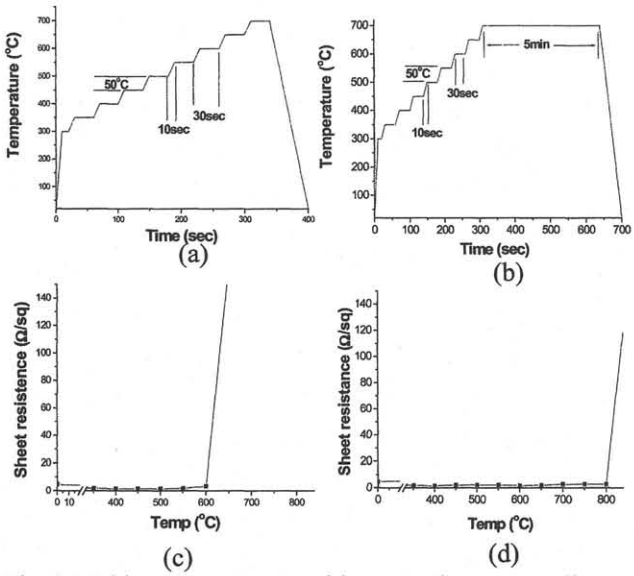

Fig. 2 Multi-step temperature history and corresponding resistance of silicide. By stretching of highest annealing temperature holding time from 30sec(a) to 5min(b), maximum temperature with low resistance increased from 600°C to 800°C.

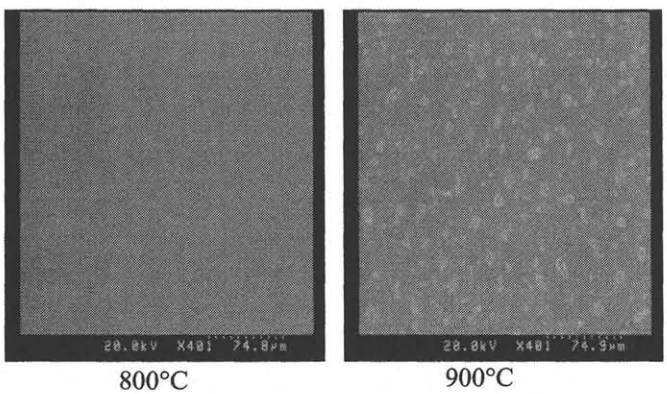

Fig. 3 SEM micrograph showing surface morphology of multi-step annealed nickel silicide with changing maximum temperature.

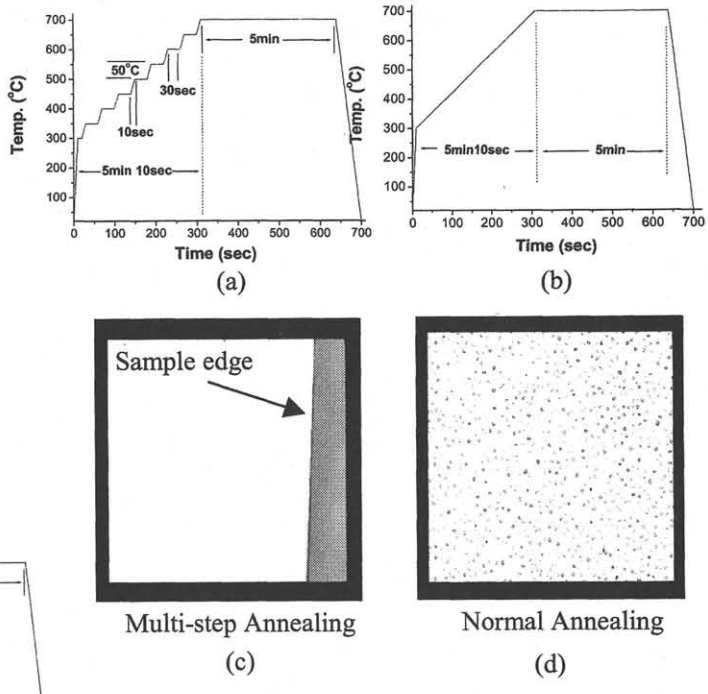

Fig. 4 Comparison between multi-step annealing and normal annealing. (a) and (b) represent the temperature histories of multi-step annealing and normal annealing, respectively. (c) and (d) show the photomicrographs of nickel silicide samples formed from 40nm thick nickel film deposited on the bulk wafer by multi-step annealing and normal annealing at 700°C, respectively.

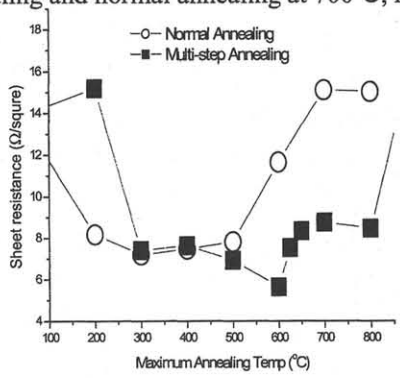

Fig. 5 Sheet resistance of nickel silicide as a function of annealing temperature comparing between multi-step annealing and normal annealing.

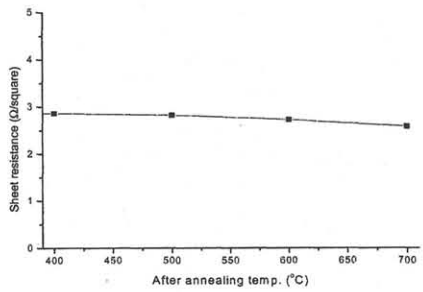

Fig. 6 Sheet resistance of nickel silicide as a function of post annealing temperature to confirm the thermal stability of composed nickel silicide.