

## Thermal Stability of HfO<sub>2</sub>/Ultrathin-SiO<sub>2</sub>/Si Structures

Noriyuki Miyata,<sup>1</sup> Masakazu Ichikawa,<sup>1,2</sup> Toshihide Nabatame,<sup>3</sup> and Akira Toriumi<sup>1,2</sup>

<sup>1</sup>MIRAI Project, Advanced Semiconductor Research Center (ASRC), National Institute of Advanced Industrial Science and Technology (AIST), AIST Tsukuba Central 4, Tsukuba, Ibaraki 305-8562, Japan  
Phone: +81-298-61-2511, Fax: +81-298-61-2642, E-mail: nori.miyata@mirai.aist.go.jp

<sup>2</sup>The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan

<sup>3</sup>MIRAI Project, Association of Super-Advanced Electronics Technology (ASET),  
AIST Tsukuba West, Tsukuba, Ibaraki 305-8569, Japan

### 1. Introduction

Thermal stability of high-*k* gate dielectrics on a Si substrate is a crucial issue for integrating these materials into the standard MOSFET, because the gate dielectrics must withstand thermal annealing, e.g. dopant activation (900-1000°C). HfO<sub>2</sub> is a prospective candidate as well as ZrO<sub>2</sub>. It is expected that the HfO<sub>2</sub> film on Si is similar in thermal property to the ZrO<sub>2</sub>. The ZrO<sub>2</sub> shows two problematic phenomena: the growth of Si oxide or silicate at the high-*k*/Si interface [1-4], and the formation of silicide at high temperature (>900°C) [2,4,5]. The former results in high EOT (equivalent oxide thickness), and the latter apparently loses the dielectric nature. Consequently, we should carefully choose the annealing conditions, but the process window for the HfO<sub>2</sub> film was not determined in detail. In this work, we examine the structural change of HfO<sub>2</sub>/ultrathin-SiO<sub>2</sub>/Si system due to the thermal annealing under various O<sub>2</sub> pressures.

### 2. Experimental

Sample preparation was carried out by using an ultrahigh-vacuum (UHV) electron-beam deposition system. Firstly an n-type Si(100) sample was heated at 900°C under the UHV conditions to expose the clean Si surface. An ultrathin SiO<sub>2</sub> layer, about 0.3 nm, was then thermally grown at 650°C in 2×10<sup>-6</sup> Torr O<sub>2</sub> for 10 minutes. The 2.6-nm-thick HfO<sub>2</sub> film was deposited on the SiO<sub>2</sub> at 400°C by using an evaporation of metallic Hf in 2×10<sup>-6</sup> Torr O<sub>2</sub>. For the thermal annealing and surface analysis, we used an UHV surface-analysis system connected with an UHV preparation chamber. The samples were annealed at 500-1000°C in 1×10<sup>-4</sup>-10<sup>-7</sup> Torr O<sub>2</sub> for 3 minutes, and then examined by using XPS (x-ray photoelectron spectroscopy), SEM (secondary electron microscopy), and μ-AES (microprobe Auger electron spectroscopy).

### 3. Results and Discussion

Figure 1 shows the typical Si 2p and Hf 4f XPS spectra observed from the annealed samples. The spectra shown in Fig 1(a) are quite the same as those for the as-grown sample (not shown), representing that the HfO<sub>2</sub>/SiO<sub>2</sub>/Si structure is stable under this annealing condition. By increasing the O<sub>2</sub> pressure, the oxide component of the Si 2p spectrum shown in Fig. 1(b) apparently increases, which was assigned to Si 4+ (SiO<sub>2</sub>). In this case, the SiO<sub>2</sub> layer

was estimated to be about 2 nm. This result was consistent with the XTEM image, showing that the 2-nm-thick SiO<sub>2</sub> grew at the HfO<sub>2</sub>/Si interface. The O<sub>2</sub>-pressure and temperature dependences of the interfacial SiO<sub>2</sub> shown in Fig. 2(a) indicate that the oxidation is sensitive to the O<sub>2</sub> pressure. It is obvious that the high vacuum conditions are required to suppress the interfacial oxidation. On the other hand, the Si 2p and Hf 4f spectra shown in Fig. 1(c) indicate that the interfacial Si oxide decomposes and the Hf silicide is formed at 900°C in 1×10<sup>-6</sup> Torr O<sub>2</sub>. Figure 2(b) indicates that the silicidation takes place at temperatures above 900°C. The gray region in Figs. 2(a) and 2(b) corresponds to the process window determined by XPS, in which the HfO<sub>2</sub>/SiO<sub>2</sub>/Si structure is stable. This result suggests that the thermal treatment of HfO<sub>2</sub> film requires the high vacuum (~10<sup>-7</sup> Torr) and lower temperature (<900°C) conditions. On the contrary, a standard MOSFET with HfO<sub>2</sub> gate dielectrics was recently demonstrated, which was fabricated by the conventional process including a dopant activation at 900-1000°C [6]. This is obviously inconsistent with the process window as determined by XPS.

Figure 3 shows the SEM image and μ-AES spectra observed from the HfO<sub>2</sub> surface annealed at 900°C in 1×10<sup>-6</sup> Torr O<sub>2</sub>. The dark circles with several tens μm in diameters are observed, which show clear Si and weak Hf

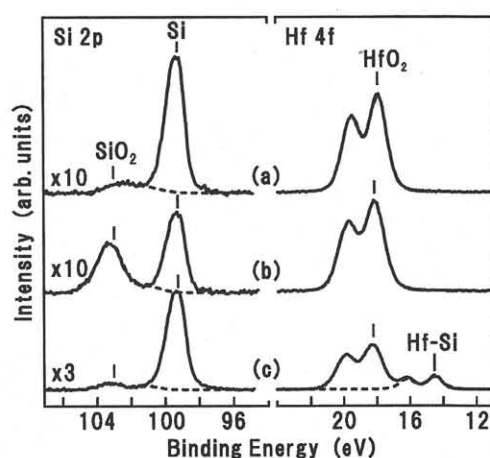


FIG.1 Si 2p and Hf 4f XPS spectra for the various annealing conditions. (a) 800°C, 1×10<sup>-7</sup> Torr. (b) 800°C, 1×10<sup>-5</sup> Torr. (c) 900°C, 1×10<sup>-6</sup> Torr.

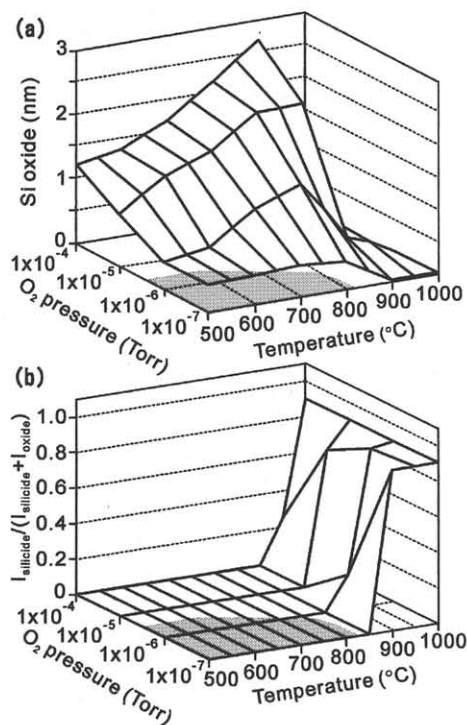


FIG.2  $O_2$  pressure and temperature dependences of (a) interfacial Si oxidation, and (b) silicidation.

AES peaks representing the formation of Hf silicide. The surrounding bright area shows clear Hf and O AES peaks, but does not show the Si peak. Thus, the  $HfO_2$  layer remains around the silicide circles. We also observed that the silicidation proceeds as a two-dimensional (2D) expansion of the silicide circles, as schematically shown by Fig. 4(a). Here, we consider the thermal stability for the case of actual MOSFET. Because the poly-Si layer that covers the  $HfO_2$  surface suppresses the  $O_2$  incorporation into the  $HfO_2$ /Si interface [4], the interfacial oxidation is expected to be suppressed. However, this poly-Si layer can not prevent the silicidation [4]. On the other hand, actual gate area of the  $HfO_2$  film is less than  $\mu m^2$ . In this case, the silicidation is also expected to be avoidable as shown by the process in Fig. 4(b). If a part of the patterned  $HfO_2$  areas has silicide nuclei, the silicidation proceeds like a case of non-patterned film, while the other parts of the patterned areas which have no nuclei remain thermally stable without silicidation, if the edge of  $HfO_2$  area is terminated by appropriate stable materials. As a result, some patterned areas survive under higher temperature annealing. In this idea, the nucleus density is an important factor which determines the probability of failure due to the silicidation. From the SEM observation, the nucleus density was estimated to be less than  $1 \times 10^3 \text{ cm}^{-2}$ . Therefore, most of sub- $\mu m^2$   $HfO_2$  patterns can survive. However, from a viewpoint of ULSI fabrication, it is obvious that the silicidation is a crucial problem. We consider that the control of silicide nucleation is essential to apply the  $HfO_2$  to ULSI devices.

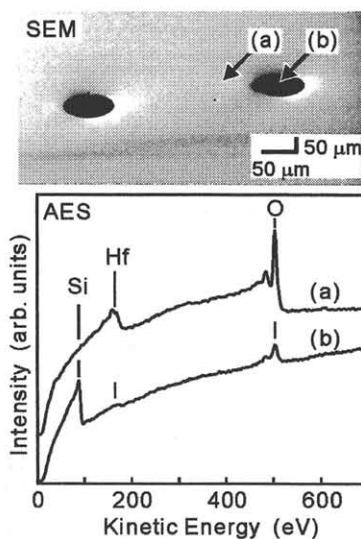


FIG.3 Formation of Hf silicide (dark area) observed by SEM and  $\mu$ -AES.

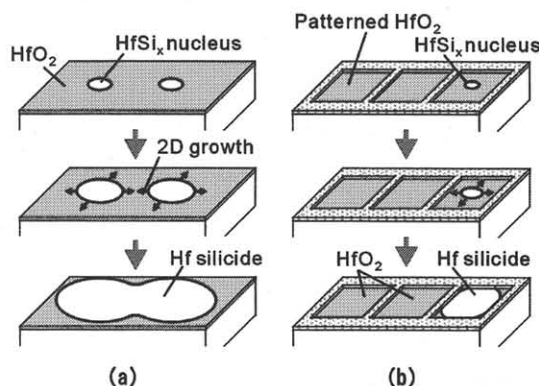


FIG.4 Silicidation for a non-patterned- $HfO_2$  layer (a) and a patterned- $HfO_2$  (b).

#### 4. Conclusion

Thermal treatment of  $HfO_2$ /Si structure requires high vacuum conditions ( $\sim 10^{-7}$  Torr) to suppress the interfacial Si oxidation. Also, the silicidation proceeds in a 2D manner at temperatures higher than  $900^\circ C$ . We suggested that the control of the silicide nucleation is important for realizing  $HfO_2$  gate stack structures.

#### Acknowledgments

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