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The Electrical Conduction of Ultra Thin SiO_2 on Slightly Iron-contaminated *p-type* Si Wafers

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1. Introduction

Metallic contamination is one of the key factors degrading the yield and the reliability of Si devices [1]. Among the metallic contaminants, iron has been extensively studied for many years, because it is commonly observed as a dissolved impurity in Si wafers and is difficult to completely eliminate during production processes. Due to technological difficulties, there are few reports on the microscopic behavior of electrical conduction of ultra thin oxide layer after slight iron contamination. Using a nanometer-scaled conductive tip working on bare gate oxide layer allows us to characterize the electrical properties of local areas of the oxide layer [2]. In this work, we have employed electrical scanning probe microscopy (SPM) to observe the individual current leakage sites, which exhibit a specific current-voltage (I-V) behavior. The dependence of the leakage behavior on iron contamination is discussed. A nitrate solution with a low iron concentration (10 ppm) has been used to contaminate *p-type* silicon wafers to simulate a real iron contamination situation under typical processing conditions.

2. Experiments

The sample preparation has been reported in our previous work [3]. Before thermal oxidation, the iron concentration on the Si wafer surface was about 10^{11} atoms/cm^2 according to total-reflection X-ray fluorescence spectrometer analysis. An electrical SPM (NT-MDT Slover P47) was employed to obtain the current images at a constant dc bias as well as the I-V curves of the leakage sites on oxide layer. Figure 1 illustrates the schematic diagram of the electrical SPM measurement. The conductive tip works on the surface of the bare oxide and the dc bias applied at back electrode ranges from -10 V to +10 V. The current sensor of the SPM system is sensitive to a signal variation as small as 1 pA. Commercially available gold-coated silicon tips were used in this work. A JEM 2010F transmission electron microscope (TEM) at a 200 kV accelerating voltage was used to measure the physical thickness of the ultra thin oxide layer.

3. Results and Discussion

Figure 2 shows the cross-sectional TEM image of the slightly iron-contaminated sample with 4 nm thick SiO_2 layer. It is evident that the iron-induced defect region exhibits an obvious strain contrast. The physical thickness of the oxide layer is uniform for the defect region and the surrounding areas. Figure 3 shows the current image at a sample bias of +10 V. It is clear that there are three leakage sites in the scanning area of about 36 μm^2. For further investigating the leakage behavior of the leakage sites, we analyzed the I-V plots of the leakage sites and the surrounding areas. The surrounding areas exhibit a leakage current level smaller than 10 pA at a sample bias ranging from -10 V to +10 V. Figure 4 (a) shows the I-V curve of the leakage site indicated by a white arrow shown in Fig. 3. The large current leakage at negative sample bias may be due to the donor type iron contaminants, which locate near SiO_2/Si interface [4] and provide the tunneling electrons at the high field regime. Figure 4 (b) shows a negative differential resistance (NDR) behavior at a sample bias of +5.72 V. This can be interpreted by trap assisted tunneling in the oxide layer [5]. Moreover, low field leakage current phenomenon has also been observed as shown in Fig. 4 (c). We believe that interface defects, including electron- and hole-traps, lead to the leakage current at low field regime. Scanning capacitance microscopy (SCM) image has revealed the existence of interface traps, which provide additional positive charges at the low field [4]. Figure 5 shows a SCM image at a sample bias of -1 V. From Fig. 4 (c) and Ref. 4, the leakage current induced by electron-traps is larger than that induced by hole-traps. Experimental results suggest that the dominant interface defects induced by slight iron contamination are electron-traps.

4. Conclusions

In summary, we have employed an electrical SPM system to study the electrical conduction of the ultra thin oxide layer thermally grown on slightly iron-contaminated p-type silicon wafers. At negative sample biases, large leakage current is detected because of the donor type iron

contaminants near the SiO_2/Si interface. Iron contamination induced interface defects, including electron- and hole-traps, lead to the leakage current at the low field regime. Experimental results indicate that the dominant interface defect is electron-traps and agree with our previous report. The negative differential resistance (NDR) behavior induced by the trap assisted tunneling has also been observed at a sample bias of +5.72 V.

References

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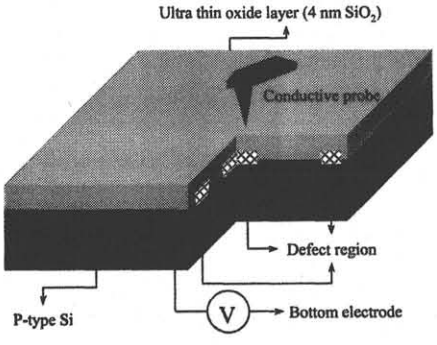

Fig. 1 Schematic diagram of electrical SPM measurements.

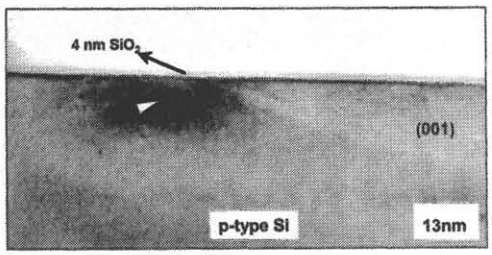

Fig. 2 The cross-sectional TEM image of the sample used in this work. A defect region with obvious strain contrast is clearly observed. The physical thickness of the oxide layer is uniform across the area examined.

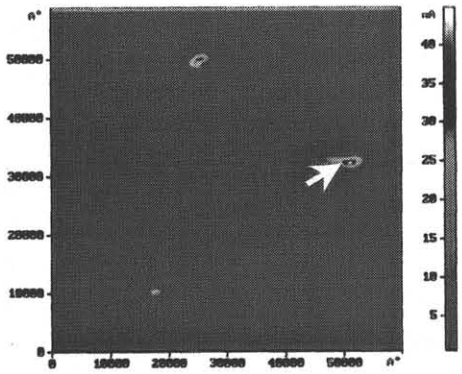

Fig. 3 The current image at an applied dc bias of +10 V. Three leakage sites were found in this scan area.

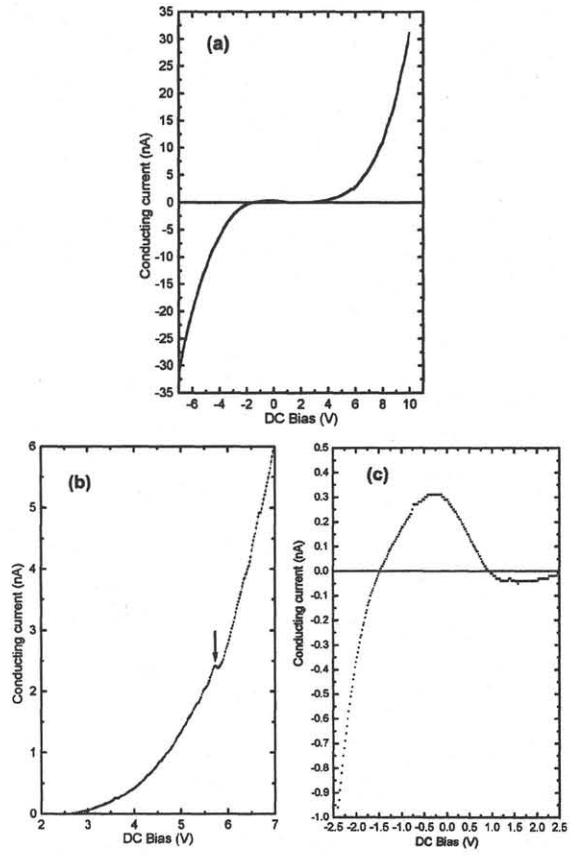

Fig. 4 (a) The I-V curve of the leakage site shown in figure 3 (white arrow). Figures (b) and (c) show NDR and low field leakage behaviors, respectively.

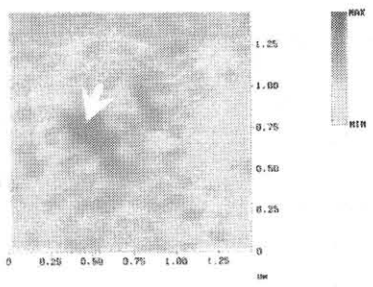

Fig. 5 The SCM image at an applied sample bias of -1 V. Due to the interface traps, the defect region (white arrow) exhibits an obvious bias-dependent contrast [4].