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Reduced Gate Leakage in AlGaAs/InGaAs pHEMTs by a Si_3N_4 Sidewall Planarized Process

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1. Introduction

AlGaAs/InGaAs heterostructure filed-effect transistors (pHEMTs) on semi-insulating GaAs substrates have successfully been applied to microwave circuit applications. However the fabrication of these pHEMTs by the conventional mesa isolation causes the gate leakage from the sidewall contacting regions, where the InGaAs channel is exposed directly to the gate feeders. This results in a low Schottky barrier height and a sidewall leakage path from the gate to channel.

Conventional Air-bridged [1~2] and selectively sidewall recessed [3] processes have been utilized in the pHEMT isolation to eliminate the contacting problem. In this report, we suppress the gate leakage from the mesa-sidewall, and increase the gate-to-drain breakdown voltage and microwave power performance by using the Si_3N_4 sidewall planarized (SSP) process. This one-step technique is automatically self-aligned to the mesa regions without requiring additional mask. The measurements of the dc and microwave power characteristics confirm the substantial elimination of sidewall leakage on pHEMTs.

2. Device structures and fabrication

The MBE-grown double hetersotructure AlGaAs/InGaAs pHEMT, shown in Fig. 1(a), consists of a 200 nm $Al_{0.2}Ga_{0.8}As$ buffer layer and a 15 nm undoped pseudomorphic $In_{0.15}Ga_{0.85}As$ channel was sandwiched by the two 3 nm undoped $Al_{0.2}Ga_{0.8}As$ spacer layer with silicon planar doped layer ($n = 5\times10^{12}$ cm^{-2}). A 35 nm undoped $Al_{0.2}Ga_{0.8}As$ was used for Schottky barrier layer and finally a 20-nm n^+-GaAs cap doped at 5×10^{18} cm^{-3} was grown to improve the ohmic contact resistivity.

Device fabrication was realized by the use of conventional lithography and lift-off techniques. Ohmic contacts were formed by electron beam evaporating Au/Ge/Ni/Au alloy, followed by a 430°C, 2 min hot plate annealing. An $NH_4OH/H_2O_2/H_20$ (3:1:100) solution was used for mesa etching to a 100 nm depth. Then before removing the mesa-level photoresist mask, a 50~60 nm Si_3N_4 sidewall protection film was deposited by a sputter (Fig. 1(a)). For comparison, the conventional pHEMTs were also fabrication without the Si_3N_4 sidewall protection. For the gate fingers and pads, Ti/Au was evaporated and lifted off. Fig. 1(b) shows an SEM photograph of finished Si_3N_4 sidewall planarized pHEMTs. This confirms the successful gate metal insulated from the channel by inserting a Si_3N_4 insulator on the sidewall region.

3. Device DC and microwave power performance

To study device sidewall leakages, we measured the Schottky gate performance of SSP-pHEMTs and mesa-pHEMTs. Shown in Fig. 2, the breakdown voltage (gate reversed current= 1 mA/mm) of SSP-pHEMT is increased from 3.8 V to 5 V, and gate turn-on voltage is also increased form 0.7 V to 0.8 V. The gate leakage current of SSP-pHEMT is significantly reduced by an order of magnitude, owing to the elimination of sidewall gate leakage path directly from the gate to low bandgap channel material.

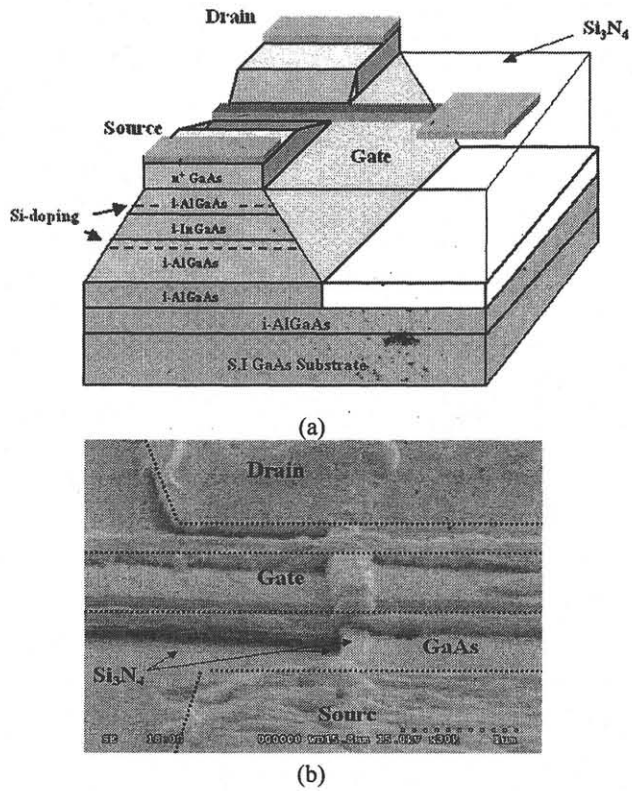


Fig. 1. (a) The perspective of the Si_3N_4 sidewall planarized AlGaAs/InGaAs pHEMT. (b) SEM photographic of the Si_3N_4 sidewall process planarized device.

Fig. 3 shows the V_{gs} dependence of transconductance (g_m) and I_{ds} curves for SSP-pHEMT and mesa-pHEMT. The maximum g_m are 255 mS/mm for SSP-pHEMTs and 175 mS/mm for mesa-pHEMTs, respectively. The I_{ds} versus V_{gs} profiles show a wider linear operational range in the forward bias of SSP-pHEMTs resulting from the lower gate-leakage and higher turn-on voltage.

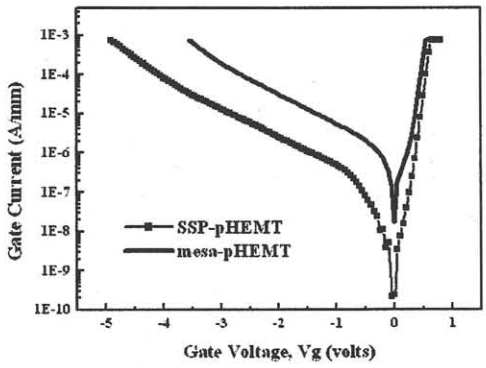


Fig. 2. Schottky diode characteristics of Si_3N_4 sidewall planarized PHEMTs (SSP-pHEMT) and conventional mesa-pHEMTs

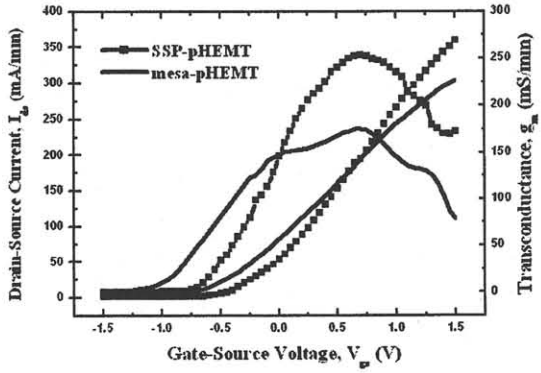
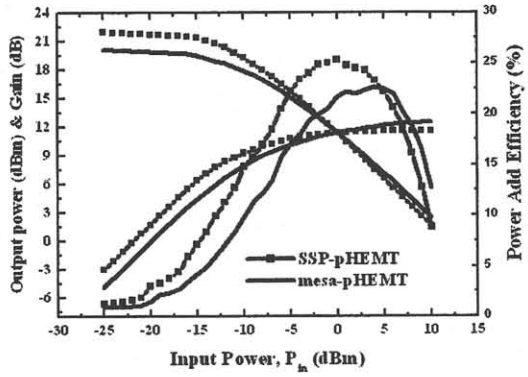
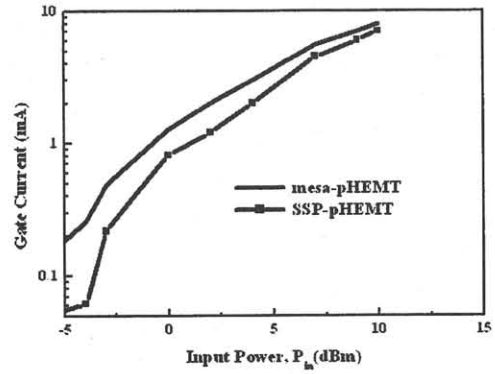


Fig. 3. Device g_m-I_{ds}-V_{gs} transfer curves characteristics of SSP-pHEMTs and mesa-pHEMTs

By extracting the on-wafer microwave S-parameters measurement, we obtained the maximum f_T (f_{max}) of 12 (34) GHz for SSP-pHEMT and 11 (30) GHz for mesa-pHEMT at V_{ds} = 3 V and V_{gs} = 0.2 V. After fitting the small-signal equivalent circuit model, we obtain the gate-to-drain capacitance C_{gd} = 0.37 pF/mm for SSP-pHEMTs and C_{gd} = 0.44 pF/mm for mesa-HEMTs. The lower-feedback capacitance C_{gd} in Si_3N_4 sidewall planarized process is certainly corresponding to the gate current reduction. Fig. 4(a) shows the microwave power measurement of both SSP-pHEMT and mesa-pHEMT at V_{ds} = 3 V and V_{gs} = 0.2 V under a 1.8 GHz operation. The linear gain is 21.9 dB with a P_{1dB} of 12.7 dBm, and max. PAE of 24% for SSP-pHEMT, while these values are 20.1 dB, 8.7 dBm and 22 % for the mesa-pHEMT. Fig. 4(b) also shows the gate leakage current versus input power levels of mesa-pHEMT is higher than that of SSP-pHEMT. Therefore, with developed Si_3N_4 sidewall planarized process in pHEMT fabrication not only shows good dc characteristics but also performs improved microwave power characteristics.



(a)



(b)

Fig. 4. Microwave power performance and gate leakage current versus input power of SSP-pHEMT and mesa-pHEMT for 1×200 μm device under 1.8 GHz operation.

4. Conclusions

We proposed a Si_3N_4 sidewall planarized process for improving device mesa sidewall gate leakage current of the AlGaAs/InGaAs pHEMTs without the extra mask design. By using this technology, we improved the device Schottky gate characteristics and microwave power performance. This technology is also suitable for the other high power devices with a low bandgap channel, such as metamorphic HEFTs and InP-based HEMTs.

Acknowledgments

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References

[1] K. Y. Hur and R. C. Compton, *IEEE Electron. Device Lett.*, **40**, 1736 (1993)

[2] H. C. Chiu, S.C. Yang, F.T. Chien and Y.J. Chan, *IEEE. Electron Device Lett.*, **23**, 1 (2002)

[3] S. R. Bahl, and J. A. del Alamo, *IEEE. Electron Device Lett.*, **13**, 1 (1992)