P5.3

Enhancement and Accumulation Mode Operation of GaAs MISFETs and InAlAs/InGaAs MISHEMTs with nm-Thin Gate Oxide Layers

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1. Introduction
For a future ultra-high-speed field-effect-type transistor, a nm-thin gate insulating layer is indispensable in order to suppress gate leakage current which associates with down sizing based upon the scaling rule [1]. This paper reports the current suppression effect of the nm-thin gate insulating layers, which are formed by direct oxidation of the semiconductor surfaces.

2. Oxide Layers
We fabricated Metal/Insulator/Semiconductor (MIS) type GaAs FETs and InAlAs/InGaAs HEMTs with single nm-order thin oxidized GaAs and oxidized InAlAs layers, both formed by UV & ozone process, as the gate insulators, respectively. The oxides thicknesses are nearly proportional to square root of the UV & ozone process periods in the single nm-range as shown in Fig. 1 [2]. The current suppression effects of the oxide layers, which were measured as the leakage current difference between fabricated MIS and Schottky diodes, are shown in Fig. 2. The oxidized GaAs and the oxidized InAlAs show nearly equal current suppression effects per thickness.

3. MISFET and MISHEMT
Based upon these results, we fabricated the MISFETs using a n/semi-insulating epitaxial wafer with 0.29 μm thickness and a donor density of 3E17/cc, and the MISHEMTs using an epitaxial wafer shown in Fig. 3. The surface pattern of the fabricated transistors is shown in Fig. 4. The gate width is 80 μm (40 μm x 2 fingers). The gate portion is recess-etched, such that about a 100 nm n-GaAs (FET) or a 10 nm InAlAs (HEMT) remain, and oxidized before forming the gate metal. A crosssectional transmission electron microscope (TEM) image of the MIS portion of a 120 min oxidated GaAs MISFET is shown in Fig. 5. A 2 – 4 nm thick amorphous oxide is observed between the single crystal GaAs and the polycrystal Al regions. Similar TEM observation of a 240 min oxidated MISFET resulted in a 6 ~ 10 nm thick oxide layer.

4. DC and RF Characteristics
Drain current vs drain voltage curves (Id-Vd), per single gate finger (40 μm width), of a 240 min oxidated 1 μm gate length MISFET, at gate voltages Vg from -2 to +3 V (0.5 V step) is shown in Fig. 6 (a). Those of 480 min oxidated and 240 min oxidated 1.5 μm gate length MISHEMTs at Vg from -1 to +4 V (0.5 V step) are shown in Fig. 6 (b) and (c). In Fig. 6 (a) and (b), maximum transconductances of 50 mS/mm (a), 38 mS/mm (b), respectively, are obtained in the accumulation mode operation (forward Vg beyond the flatband voltage (1 V)) due to over recess etching, although the small transconductance in the Vg = 0 ~ 1 V region suggests some surface related problems. These high forward Vg operations suggest effectiveness of the nm-thin oxidized GaAs/InAlAs as the current suppression layers. While in Fig. 6 (c), 250 mS/mm is obtained in the enhancement and light accumulation mode region. This high transconductance is attributed to the remained highly-doped InAlAs beneath the insulating layer. On wafer S-parameter measurement of the MISFETs were carried out and the stability factor K, the maximum stable gain MSG, the maximum available gain MAG, the unilatetal gain U, and |h21| were calculated. The RF performance of the GaAs MISFET at Vd = 4 V and Vg = 1 V is shown in Fig. 7. A current gain cutoff frequency fT of 6 GHz and a fmax of 8 GHz are obtained.

5. Conclusions
Experimental results clearly show the effectiveness of the nm-thin oxidated GaAs and InAlAs layers in suppressing the gate leakage currents, although they also suggest existing of remaining problems.
Fig. 1 Oxide thickness vs oxidation period

Fig. 2 Current suppression vs insulator thickness.

Fig. 3 Surface pattern of a MISHEMT

Fig. 4 Epitaxial wafer of the InAlAs/InGaAs MISHEMT

Fig. 5 Transmission electron microscope image of MIS portion of a GaAs MISFET with 120 min oxidized layer.
(by courtesy of Mr. K. Higashimine, JAIST)

Fig. 6 Id-Vd curves of a GaAs MISFET (left (a)) and MISHEMTs (center (b) and right (c)).
Vg = -2 - 3 V (a), -1 - 4 V (b) and (c), 0.5 V step.

Fig. 7 RF performances of a GaAs MISFET

Acknowledgement
The authors are grateful to Prof. N. Ohtsuka and Mr. K. Higashimine of JAIST for supplying the TEM images, and to Mr. A. Inoue and Mr. S. Nakatsuka for supporting the RF measurement.

References