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Evaluation of lattice distortion with nanometer resolution in Si single-electron transistor

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1. Introduction

A single-electron transistor (SET) is the most promising candidate for future electronic devices [1-3]. A Si nanowire patterned by electron beam lithography is converted into a SET by a peculiar fabrication method called pattern-dependent oxidation (PADOX). In previous work [4], SEM observation combined with electrical measurement revealed that a SET island together with tunnel barriers at both sides is made in the oxidized Si nanowire in a self-aligned manner. Though the theoretical model of Si-SET [5] predicts that the SET island is generated by oxidation-induced stress at the central part of the Si wire and the rest of the wire acts as tunnel barriers, this has not been confirmed experimentally yet. This is because the distortion in the oxidized Si nanowire is difficult to evaluate with nanometer resolution.

In this work, we observed the cross-section of one of our SET by using transmission electron microscopy (TEM). The distribution of the lattice distortion in the device was successfully evaluated from the high-resolution lattice image.

2. Sample structure

The sample for TEM observation was a SET fabricated by PADOX. The electrical properties of the sample had been measured before the TEM observation. Clear Coulomb oscillations were observed at 25 K. The gate capacitance of this device was 0.225 aF. A top-view of the structure of the embedded Si-wire in the device was observed by "see-through" SEM after removing the poly-Si gate electrode [6], as shown in Fig. 1(a). The effective length of the single electron island was measured from the relationship between the length of Si wire and the gate capacitance, as reported at SSDM2001 [4]. The length of the Si wire was 38 nm and the effective island length was 15 nm, as illustrated in Fig. 1(b).

3. TEM image of SET

The TEM sample for the cross-sectional observation was fabricated by a focused ion beam (FB2000A, Hitachi) combined with micro-sampling technology. The high-resolution TEM image was taken with an H9000 (Hitachi) at 300 kV.

Fig. 2 shows the cross-sectional TEM image of the sample. The observation area of Fig. 2(a) is the same as that of Fig. 1. Fig. 2(b) is the high-resolution image of the center of

the device. The Si lattice image in the Si wire is clearly observed.

4. Distortion in the SET device

For the quantitative measurement of the lattice distortion with nanometer resolution, we developed a new method of measuring the lattice spacing. The TEM image is averaged along the perpendicular directions of $[111]$ and $[1\bar{1}\bar{1}]$. The intensity profiles of the averaged image are shown in Fig. 3. The peaks correspond to the lattice plane of (111) and $(1\bar{1}\bar{1})$. The distribution of the lattice spacing averaged for 20 planes is plotted in Fig. 4. The lattice spacing is normalized by the value at the right edge of the image. The lattice distortion is observed at the central part of the Si wire. This is the first quantitative evaluation of the lattice distortion with nanometer resolution in Si single-electron transistor.

The length of the distorted area is about 20 nm. This value is consistent with the island length measured from the electrical properties shown in Fig. 1(b). This strongly suggests that the single electron island in the Si SET fabricated by PADOX is generated by the lattice distortion. The effect of the band-gap reduction induced by the distortion forms the single-electron island [5]. The oxidation-induced stress plays an important role in Si-SETs.

5. Conclusions

The lattice distortion in Si SET fabricated by PADOX has been evaluated from a high-resolution TEM image of the cross-section of the device. The distribution of the distortion was successfully measured with nanometer resolution. The central part of the embedded Si wire is distorted by PADOX. The length of the distorted area is almost the same as that of the single electron island estimated from the electrical properties. These results are consistent with the theoretical model of the SET device.

References

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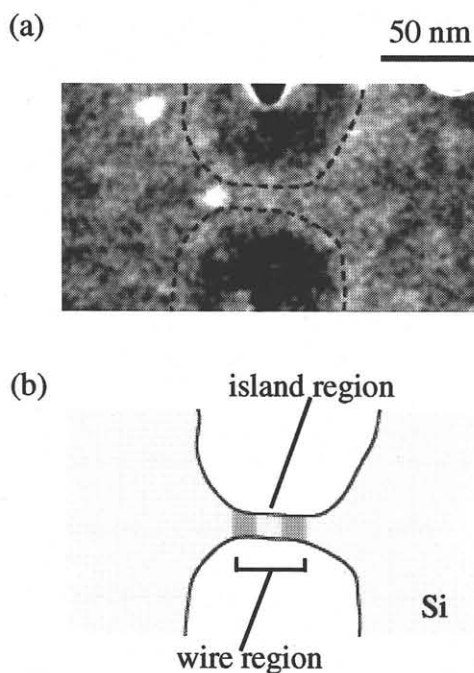


Fig. 1. Top view of the sample structure. (a) "See-through" SEM image of a SET whose electrical properties were known. An embedded Si structure is observed through the oxide layer. SET operation of this device was confirmed by electrical measurement at 25 K. The outline of the embedded Si is represented by dotted lines. (b) The outline of the embedded structure. The SET island region was estimated from the relationship between the length of the wire length and the gate capacitance of the SET.

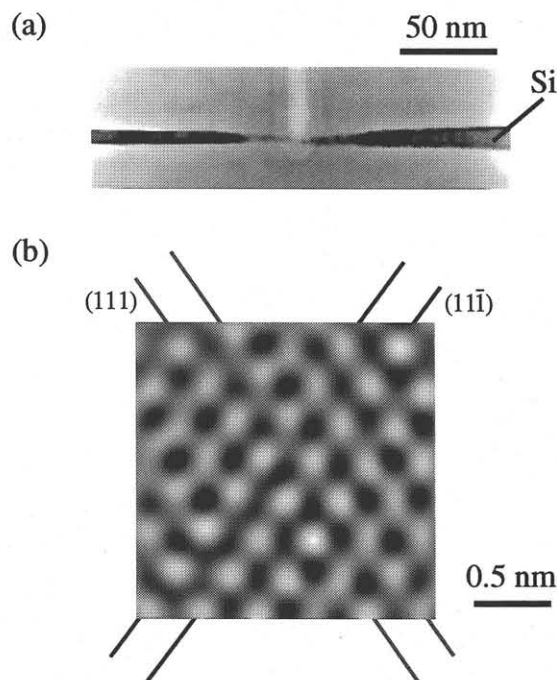


Fig. 2. TEM micrograph of the cross-section of the SET. (a) Side view of the embedded Si structure. The observation area is the same as in Fig. 1. (b) High-resolution image of the central part of the device. The (111) and $(1\bar{1}\bar{1})$ lattice planes are illustrated.

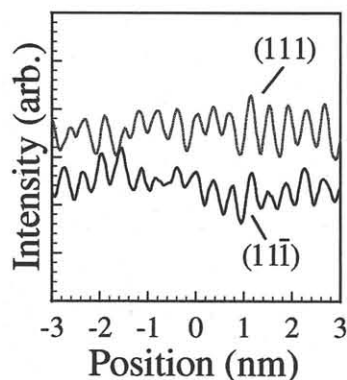


Fig. 3. The averaged intensity profile of the center of the TEM image for (111) and $(1\bar{1}\bar{1})$ planes. The peaks represent the lattice planes.

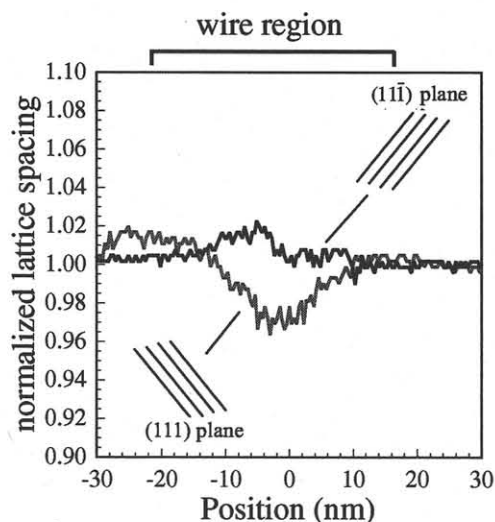


Fig. 4. The distribution of the normalized lattice spacing. The central part of the wire region is distorted by the oxidation-induced stress.