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Fabrication and characterization of a single electron transistor using n^+ GaAs

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1. Introduction

Single electron transport through semiconductor quantum dots is intensively investigated due to its interesting physics and potential applications [1]. However, most of the quantum dots (QDs) using compound materials have been fabricated by the split gate technique [2]. In this paper, we report the fabrication and the characterization of a single electron transistor (SET) made from a thin layer of n^+ GaAs. Clear Coulomb oscillations and Coulomb staircases are observed and the data are consistent with the lithographic dimension of the dot.

2. Experiment

Figure 1 (a) shows the schematic diagram of the wafer grown in a molecular beam epitaxy system. A 0.5 μm thick GaAs buffer layer, a 10 nm n^+ GaAs channel layer with the doping density of 3×10^{18} cm^{-3}, and a 30 nm GaAs cap layer were grown on a semi-insulating GaAs substrate. We used electron beam lithography and simple wet etching process to fabricate the QD and the tunnel barriers. Figure 1 (b) shows the scanning electron microscope (SEM) image of the active region. After the formation of active region we evaporated the Ti/Au gate on top of the active region for potential control of the QD. Figure 1 (c) shows the schematic of the fabricated final device structure.

3. Result and Discussion

Figure 2 shows a typical result of the drain current – control gate voltage (I_{DS}-V_{CG}) characteristics measured at 4.2 K. The value of the drain-source bias (V_{DS}) changes from 0.1 mV to 0.5 mV with 100 μV steps. There are clear Coulomb oscillations and they beat with two different periods (4.5 and 41 mV). Most probably, there will be an unintentional dot in the channel layer mainly due to random distribution of dopants, which often occurred in highly doped channel layers [3]. Figure 3 shows the 4.2 K I_{DS}-V_{DS} and the differential conductance (dI_{DS} / dV_{DS})-V_{DS} curves at V_{GS} = - 512 mV. Clear Coulomb staircases can be seen both in the I_{DS} – V_{DS} and in the dI_{DS}/dV_{DS} – V_{DS} curves. Small staircases in the middle of the staircase are probably caused by the unintentional dot. Figure 4 shows the Coulomb oscillations measured in the range $4.2 < T < 77$ K. The oscillations with the large period (41 mV) are clearly seen at $T < 10$ K and they persist up to 77 K. The observed periodicity and the T dependence are consistent with the diameter with the fabricated dot. From the larger oscillation period observed in Fig. 2 (ΔV_{GS} = 41 mV), the gate capacitance (C_G) between the gate and the dot is estimated to be 3.9 aF. From the Coulomb gap the junction capacitance C_D+C_S is estimated to be 16.2 aF. Then the total capacitance of the dot (C_Σ= $C_D+C_S+C_G$) is 20.1 aF. This leads to a dot diameter of 43.3 nm. This value is consistent with the lithographic dimension of the fabricated dot considering the depletion width of 6.7 nm. From the simple Coulomb blockade model, the charging energy was estimated to be 7.96 meV, which corresponds to the T of 92.2 K.

4. Conclusions

This paper reported the fabrication and the characterization of the SET fabricated from a thin layer of n^+ GaAs. We used electron beam lithography and one step wet etching process to obtain the small quantum dot. Clear coulomb oscillations were observed and they persisted up to 77 K. The periodicity and the T dependence are consistent with the fabricated dot diameter. There are beatings in the Coulomb oscillations at low T and they are explained by the existence of unintentional dots due to random impurity distribution in the n^+ layer.

Acknowledgments

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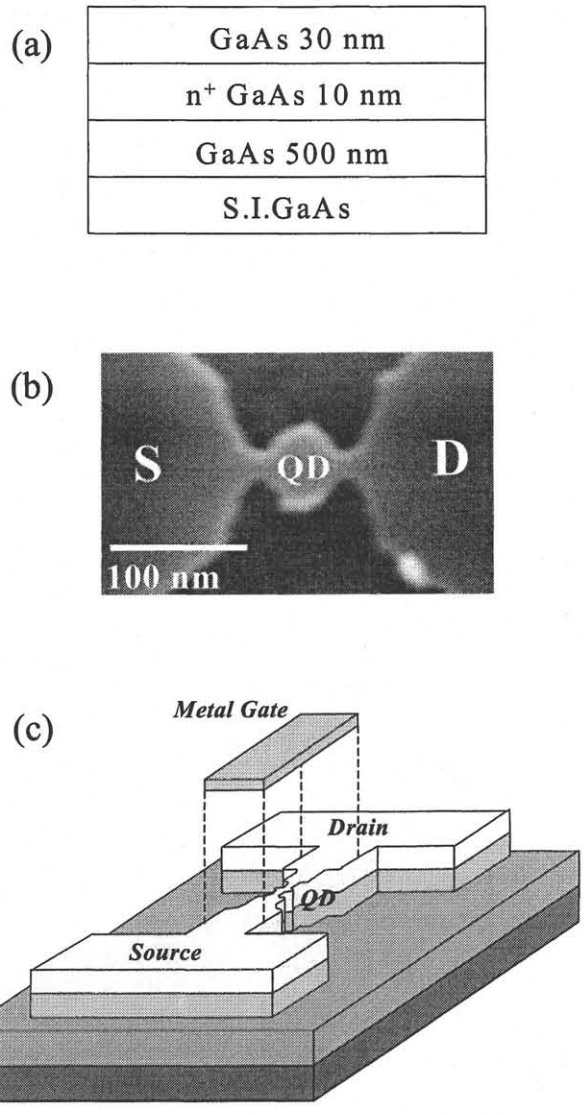

Fig. 1 (a) Schematic diagram of the wafer used in this experiment. (b) SEM photo of magnified image of the active region. (c) Schematic of the fabricated final device structure.

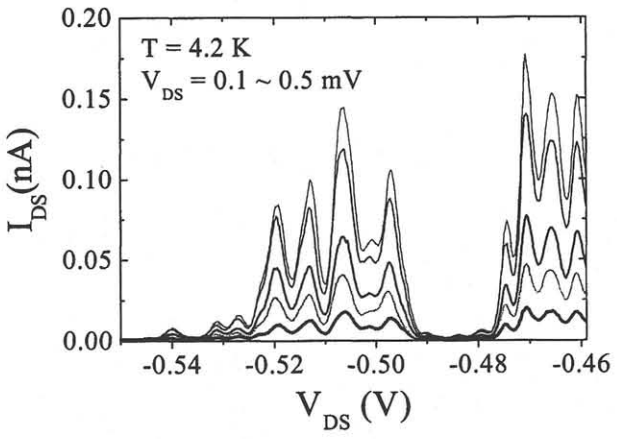

Fig 2 The I_{DS}-V_{GS} characteristics measured at 4.2 K and at several different V_{DS} Values.

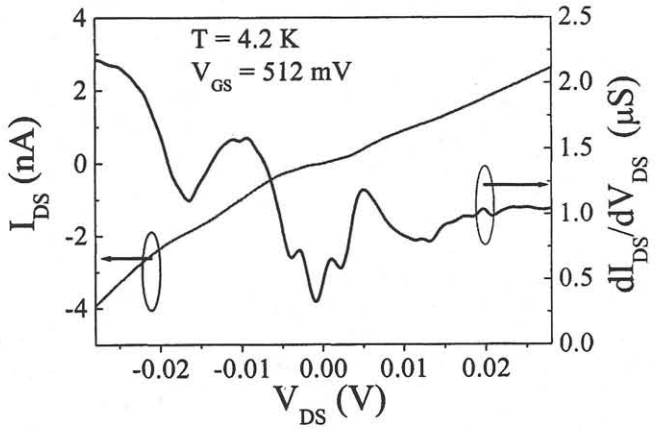

Fig 3 The I_{DS}-V_{DS} and the dI_{DS}/dV_{DS} -V_{DS} characteristics at 4.2 K.

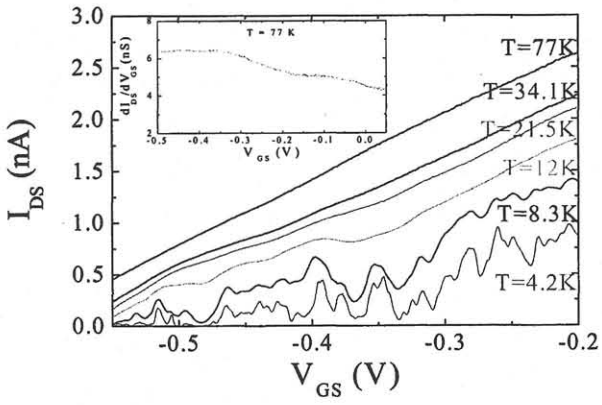

Fig 4 Temperature dependence of I_{DS} from 4.2 K to 77 K.