

## Cryogenic operation of diamond surface-channel electronic devices.

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Diamond is a promising semiconductor material for the future electronics. Owing to its high break down field (107 V/cm), extremely high thermal conductivity (20 W/cmK), high hole mobility (1800 cm<sup>2</sup>/Vs) and low dielectric constant (5.7), diamond is expected as a candidate for high power, high-frequency devices. However, room temperature device operation is still problematic in impurity-doped (boron for p-type, phosphorus or sulfur for n-type) diamond due to their deep activation energy. In that sense, hydrogen-terminated diamond is attractive for electrical applications because it induces p-type surface conduction even if the diamond is not intentionally doped. Up to now, the fabrication and the operation of MESFETs and MISFETs have been demonstrated using a surface conductive layer [1].

On the other hand, cryogenic operation of the semiconductor devices is an interesting issue not only for studying the physical properties of semiconductor materials and devices, but also for practical aspects. Expected advantages of low temperature operation of electronic systems are higher device performance because of increased carrier mobility and saturation velocity, lower power dissipation because of the sharper turn-on characteristics of FETs, reduced thermally activated degradations of the device performance

and so on. To investigate the carrier behavior of the surface conductive layer at low temperature, and to elucidate the mechanism of the surface conductive layer, we demonstrated the low-temperature (~ 4.4 K) operation of the diamond FETs. Moreover, we also fabricated in-plane-gate FET structure and in-plane-gate single-electron transistor on diamond surface, and cryogenic operations are performed.

DC characteristics of a 5 μm-gate Cu/CaF<sub>2</sub>/diamond MISFET are shown in Fig. 1. FET operates successfully at cryogenic temperature, even though the carrier freeze-out below the specific critical temperature was reported in diamond surface conductive layer [2]. In the DC characteristic at 4.4 K, drain current suppression occurs at  $V_{GS}=0$ , which is related to the carrier freeze out. However, in the FET structure, carrier can be induced by the sufficient field effect (field effect doping). In the low-temperature characteristics, we have to consider the drain threshold voltage which appears at  $V_{DS}\sim 0.3V$ . This is due to the energy barrier existing between the source/drain electrode and the surface conductive layer. At 300 K, carriers have enough thermal energy to overcome such barrier. However, at low temperatures, this small potential barrier is higher than thermal energy of carriers. This barrier is remarkably reduced by the longitudinal electric field that results from the drain bias  $V_{DS}$ .

Figure 2 shows the transconductance vs. gate voltage characteristics of the MISFET. Maximum transconductance slightly increase from 300 K to 77 K, and reaches 14.5 mS/mm at 4.4 K. Calculated channel mobility increases from 97  $\text{cm}^2/\text{Vs}$  to 190  $\text{cm}^2/\text{Vs}$  as temperature drops down to 4.4 K. This transconductance increase at low temperature is due to the reduced phonon scattering. Furthermore, Coulomb scattering from the ionized impurity etc. existing at subsurface region is also reduced due to the electric screening by the accumulated charge.

Figure 3 shows the  $V_{GS}$ - $I_{DS}$  characteristic of the in-plane-gate single-electron transistor fabricated by AFM-anodization technique [3]. Clear single-period current oscillation with good peak-to-valley ratios is observed by optimizing the

quantum dot formed by the gate-driven carrier depletion.

## References

- [1] H. Umezawa, H. Taniuchi, T. Arima, M. Tachiki, K. Tsugawa, S. Yamanaka, D. Takeuchi, H. Okushi and H. Kawarada, *Jpn. J. Appl. Phys.* **39**, L908 (2000).
- [2] C. E. Nebel, C. Sauerer, F. Ertl, M. Stutzmann, C. F. O. Graeff, P. Bergonzo, O. A. Williams and R. A. Jackman, *Appl. Phys. Lett.* **79**, 4541 (2001).
- [3] M. Tachiki, T. Fukuda, K. Sugata, H. Seo, H. Umezawa and H. Kawarada, *Jpn. J. Appl. Phys.* **39**, 4631 (2000).

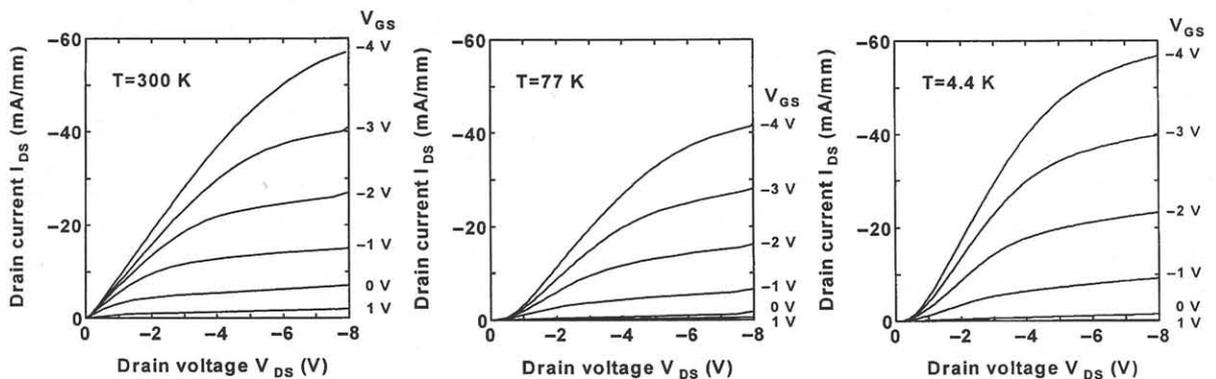


Fig.1 Static characteristics of 5  $\mu\text{m}$ -gate Cu/CaF<sub>2</sub>/diamond MISFET.

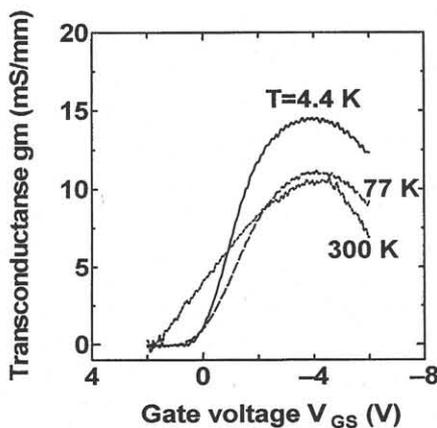


Fig. 2. Transconductance vs. gate voltage characteristics of the MISFET.

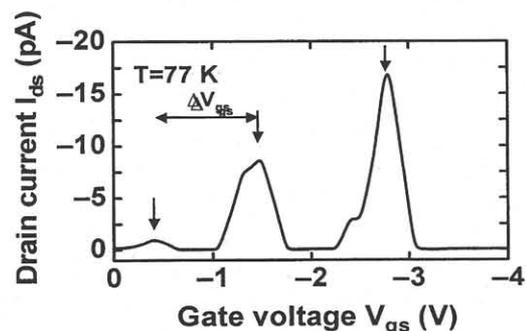


Fig. 3.  $V_{GS}$ - $I_{DS}$  characteristic of a diamond single-electron transistor at 77 K. The  $V_{DS}$  is - 50 mV.