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Manufacturability of High-Voltage Circuits on thin-film SOI

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1. Introduction

The advantages of Silicon-on-Insulator (SOI) for low-power and high-speed circuits are well known [1]. The advantages of dielectric insulation have also been applied to power-integrated circuits, both for thick-film [2] and thin-film [3] SOI. Recently, a theoretical study demonstrated the power density (specific on-resistance vs. rated breakdown voltage) of thin-film SOI to be comparable with super-junctions [4], and well ahead of other technologies. The objective of this paper is to show manufacturability of such thin-film SOI processes for 24-650V circuits in volume production.

2. Motivation

Background

The drive to decrease size, increase efficiency, and further improve reliability of power-conversion circuitry motivates a transfer from solutions with discrete components to an integrated approach. Progress towards this goal was delayed by problems of incompatibility between control circuits and power-devices on the same chip, as well as potential interrelations, such as latch-up by minority carrier generation or injection in power devices. Furthermore, economies of custom-designed ICs compare unfavorably with off-the-shelf standard products. The former roadblock is resolved by dielectric isolation with SOI, whereas the latter requires aggressive reduction of device and circuit size.

Alternatives

Most power-device architectures (VDMOS, HEXFET, Trench-FET, super-junctions) do not lend themselves to circuit integration. This is due to the fact that the high-voltage terminal is usually at the back-side of the wafer, making multiple high-voltage terminals impossible. This problem can be resolved by integrating the devices in thick-film SOI, but the contacting of the buried high-voltage terminal will introduce additional parasitic resistance and capacitance.

Lateral device concepts, such as RESURF [5], bring the high-voltage terminal to the front, and electrical isolation is possible by reverse-biased junctions and self-terminated geometry. A potential problem remains with high displacement currents invoked during switching of a power device. Furthermore, inherent n-p-n-p structures can be triggered to latch-up by biasing or signal transients.

Chosen approach

Thin-film SOI combines the advantages of lateral architecture and dielectric isolation. Circuit size can be minimized by near-ideal electric field throughout the device [4] by separating the field to deplete the silicon from the field required to build the blocking voltage, see Fig. 1. Additionally, device area can be reduced, compared to other approaches, and the process can be designed to be compatible with standard CMOS components.

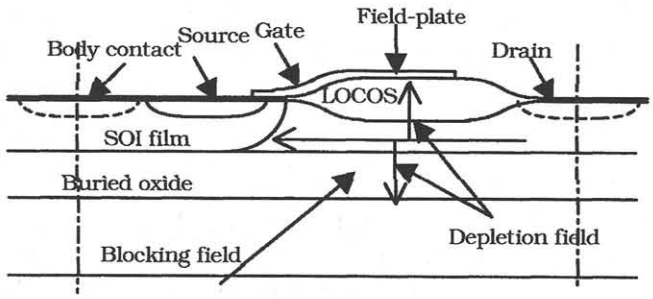

Fig. 1 Thin-film SOI power device.

3. Process introduction

Processing issues

There was quite some concern that the buried oxide under the SOI layer will adversely influence process steps. Specifically, plasma-etch and –deposition, or ion implantation could charge up the SOI layer and modify uniformity or throughput rate. We were able to virtually eliminate these effects by a proprietary protection scheme in the saw-lanes [6]. Furthermore is the considered thickness of the SOI layer (1.5um) partially transparent to visible light, therefore lithography exposure dose had to be adjusted. Metrology and visual inspection had to use shorter wavelength where the attenuation of the SOI layer is better.

Gate-oxide integrity

SOI has the reputation of suffering from lower gate-oxide quality compared to bulk processes. Attention to many processing details helped to improve this to a level very close to bulk material, see Figure 2.

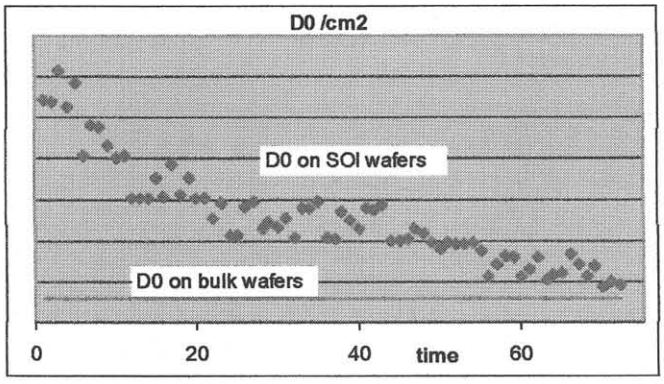

Fig. 2 Defect density reduction in SOI over time.

Key aspect for improving gate-oxide quality is the reduction of mechanical stress in silicon, as the thinner material demonstrates more rapidly slips and stacking faults. Furthermore, the contamination level has to be lowered compared to bulk processing, as known gettering techniques can be less effective in SOI [7].

Power dissipation

A point of concern in SOI is the two orders of magnitude lower thermal conductivity of oxide, compared to silicon. It has been shown earlier that ESD pulses are sufficiently rapid that only the SOI layer is involved in heating by the dissipated energy, the buried oxide has therefore no influence [8]. On the other side, the oxide just represents an additional thermal resistance of the order of the silicon wafer itself for continuous dissipation, and is therefore easily accounted for by simulation. Recent work [9] has shown slow signals to be most critical for SOI, as the equivalent thermal R-C network allows for significantly higher peak temperatures and swings than bulk material. These aspects have to be properly modeled and taken into consideration during circuit design.

Electromagnetic compatibility (EMC)

The lower parasitic capacitance in SOI permits the use of smaller signal currents, which reduces emission of high-frequency radiation. This eases EMC considerations e.g. in automotive applications [10].

4. Results

The improvements in defect density, yield, and die size reduction allowed the introduction of several applications into volume production. They cover automotive (up to 80V), audio, such as class-D amplifiers (up to 120V), drivers for electro-luminescent displays (up to 150V), Plasma-Display-Panel drivers (up to 200V), video amplifiers (300V), switched-mode power supplies and lighting applications (up to 650V). An example for such ICs is given in Figure 3.

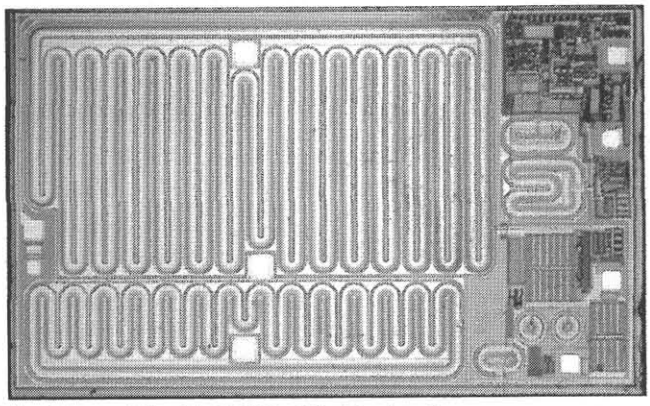
Fig. 3 Power-IC with 550V half-bridge topology.

5. Conclusions

This paper presented the introduction of thin-film SOI for power integrated circuits into volume production. SOI-specific concerns, such as plasma-induced charging, limited attenuation of light, gate-oxide integrity, and power dissipation were discussed in detail. Several applications in the range from 80V to 650V are presented.

Acknowledgments

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