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Parasitic Effects of Thin SOI MOSFETs with Body Contacts

Hongchin Lin and Jemin Lin
Department of Electrical Engineering, National Chung-Hsing University, Taichung, Taiwan
Phone: 886-4-2284-0687 ext. 250 e-mail: hclin@dragon.nchu.edu.tw

1. Introduction

Many different types of SOI MOSFET's have been proposed. Among these, the fully depleted SOI MOSFET is the most popular one, which exhibits high current drivability [1], attenuated short-channel effects [2], and enhanced immunity to hot carrier degradation [3]. However, the floating body of an SOI MOSFET results in other problems, such as drain current kink effect, low breakdown voltage [4], latch effect due to the lateral parasitic BJT [5]. Even though fully depleted SOI can reduce the kink effect, very thin Si film may lead to parasitic BJT effects. Thus, intermediate Si film thickness [6] still exits the kink effect.

In order to improve the characteristics of SOI MOSFETs, inclusion of the body contact in the device is the best solution. The body contacts can be also applied to DTMOS [7,8], in which the gate and the body are tied together for ultra low voltage/low power applications. Several body-fixed structures have been proposed. Here, we select the same T-gate and H-gate type structures proposed in Refs. [9,10]. Through investigation of body current, it was found that extra leakage current was generated due to band-to-band tunneling near the P+ body region below the gate edge.

2. Device Structure and Fabrication

Fig. 1 shows the top views of H-gate and T-gate SOI nMOSFETs. The channel width (W) and Length (L) are labeled in the H-gate structure. There are two extensions with width (Wx) and length (Lx) illustrated in the same figure. The reason to make the extensions is to reduce junction capacitance at the source/drain regions and simplify the process complexity.

The process conditions are the same as those reported in Refs. [9,10] and briefly described below. N+ poly silicon gate nMOSFETs were fabricated on boron doped ⟨100⟩-oriented wafers with buried oxide thickness of 400nm and silicon film thickness of 190nm. LOCOS was able to fully consume the active silicon layer in the isolation region. Channel implant was performed by BF_2 (50 keV, $6\times10^{12}cm^{-2}$), followed by 4nm gate oxide growth. After 200-nm poly-Si gates were generated, a shallow N+ S/D extension implant with As (5 keV, $1\times10^{15}cm^{-2}$) and TEOS spacers were performed. Then, As with 10 keV and $5\times10^{15}cm^{-2}$ was used for N+ S/D implant.

3. Measurement Results

To avoid complexity of short and narrow channel effects [9,10], the H-gate SOI MOSFET with W=100μm and L=20μm was used in the following analyses. The width (Wx) and the length (Lx) of the gate extension in Fig. 1 are 10μm and 5μm. Another sample with 140nm Si film thickness has the similar characteristics with slightly higher drain and body currents, so it is not discussed here.

Fig. 2 gives the normal Id-Vd curves with the body tied to the source and Vgs=1V to 4V. The threshold voltage is about 1.1V and the kink effect is effectively inhibited. Fig. 3 shows body current versus gate voltage for Vds=1V to 4V and Vbs=0. For each curve, the first hump is due to impact ionization. However, after the hump, the body current increases almost exponentially and then saturates, unlike the conventional substrate current, which is diminished as Vd is increased. This phenomenon can be explained by cutting the H-gate device in Fig. 1 along *a-a'* and shown in Fig. 4. When Vg is increased, the inversion layer is formed below the gate. If the source is floated, the lateral electric field of inversion layer near the body will be very strong. It provides the possibility of band-to-band tunneling between the P+ body region and the inversion layer.

To confirm it, measurement of Ib versus Vg for Vd=0.5V to 2V, Vb=0 with the source node floated. Fig. 5 shows the similar trend in Fig. 3. The magnitude in Fig. 5 is about 4 to 5 times larger. The reason may be due to the lateral electric field in the inversion near the source is much smaller if Vs=0, which reduces the parasitic tunneling current shown in Fig. 4. For further verification, Fig. 6 demonstrates Ib versus Vg at Vd=3V for H-gate and T-gate using the bias methods of Figs. 3 (4 electrodes) and 5 (3 electrodes). For normal operations denoted by open marks, the humps of Ib of H-gate and T-gate devices are very close, but the exponentially increased Ib of H-gate device are about twice of T-gate device due to one more gate extension of H-gate device. The floating source measurement denoted by solid marks also has the similar relationship.

4. Conclusions

The parasitic effects of SOI MOSFETs with body contacts using H- and T- type structures were investigated. Leakage current from the gate extensions due to tunneling was confirmed by floating source measurement. It is suggested that reduction of extension width (Wx) may help reduce leakage current but complicate the processes, especially for ultra short channel devices.

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References

[1] J. C. Sturm, K. Tokunaga, and J. P. Colinge, *IEEE Electron Device Lett.*, vol. 9, p. 460 (1988)
[2] T. Sekigawa and Y. Hagashi, *Solid-State Electronics*, no. 27, p. 827 (1984)
[3] J. P. Colinge, *IEEE Trans. Electron Devices*, vol. 34, p. 2173 (1987)
[4] K. Young and J. A. Burns, *IEEE Trans. Electron Devices*, vol. 35, p. 426 (1988)
[5] C.-E. D. Chen, *et al*, *IEEE Electron Device Lett.*, vol. EDL-9, p. 736 (1988)

[6] F. Balestra, t. Matrumoto, M. Tsuno, H. Nakabayashi, Y. Inoue, M. Koyanagi, *Electronics Lett.*, vol. 31, p. 326 (1995)
[7] W. Jin, P. C. H. Chan, and M. Chan, *IEEE Trans. Electron Devices*, vol. 45, p. 1717 (1998)
[8] V. Ferlet-Cavrois, P. Paillet, O. Musseau, J. L. Leray, O. Faynot, C. Raynaud, J. L. Pelloite, *IEEE Trans. Nuclear Science*, vol. 47, P. 613 (2000)
[9] S. J Chang, C. Y. Chang, S. D. Wu, T. Y. Huang, T. S. Chao, *Ext. Abst. SSDM*, (2000) p. 482.
[10] C. Y. Chang, S. J Chang, T. S. Chao, S. D. Wu, T. Y. Huang, *IEEE Electron Device Lett.*, vol. 21, p. 460 (2000)

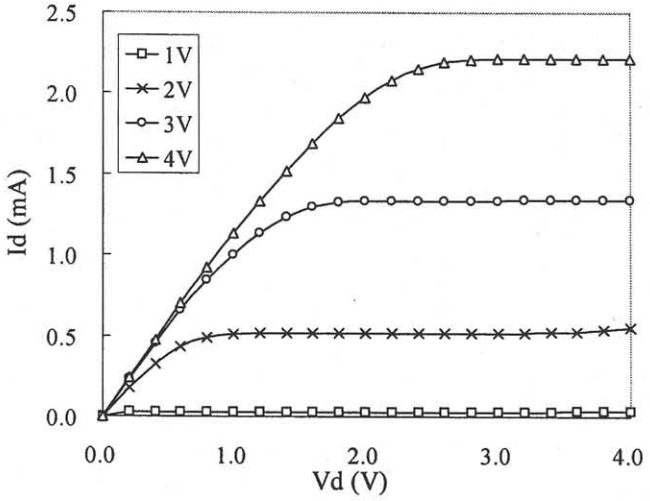

Fig. 2 The drain current indicates normal operation of the H-gate device.

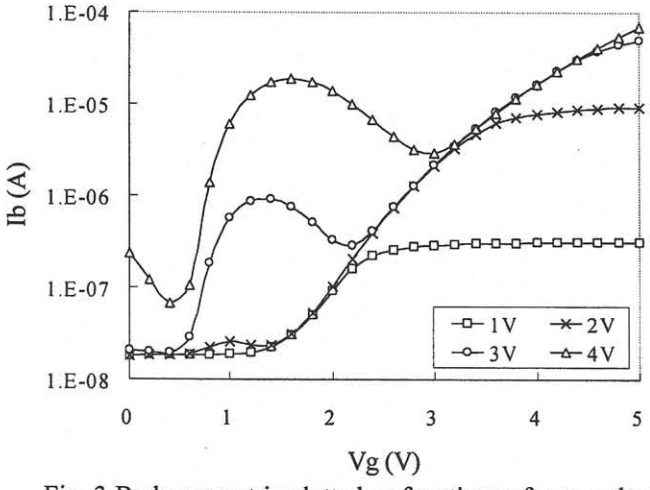

Fig. 3 Body current is plotted as functions of gate voltage when the source and the body are grounded.

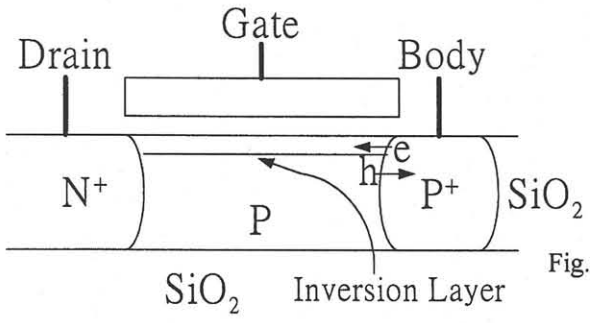

Fig. 4 Illustration of body current due to parasitic tunneling current between the inversion layer and the P+ region

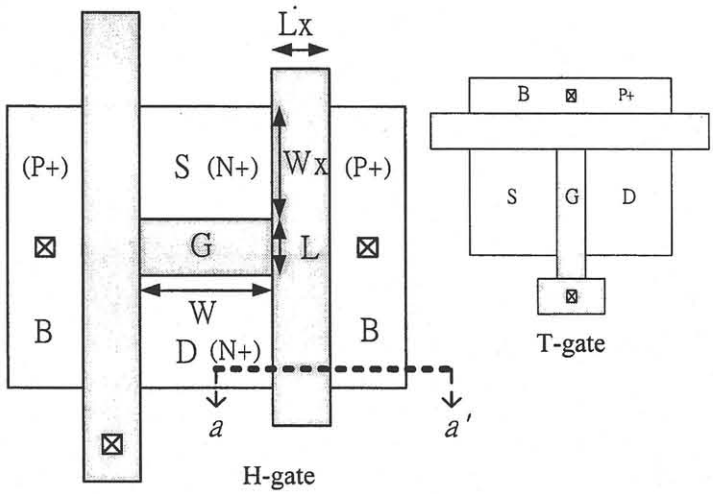

Fig. 1 The top views of H-gate and T-gate SOI MOSFETs

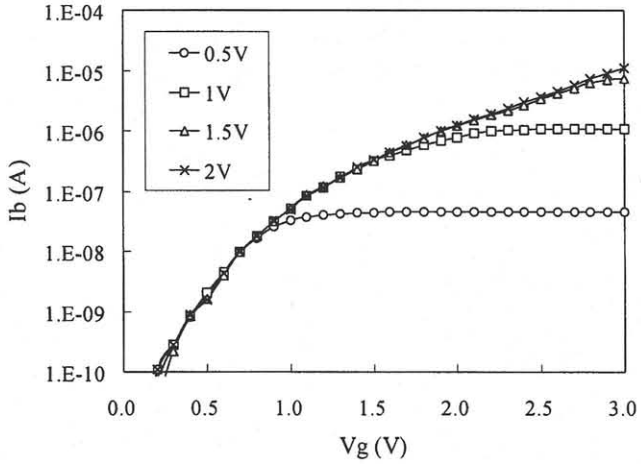

Fig. 5 Body current is plotted as functions of gate voltage when the source is floated and the body is grounded.

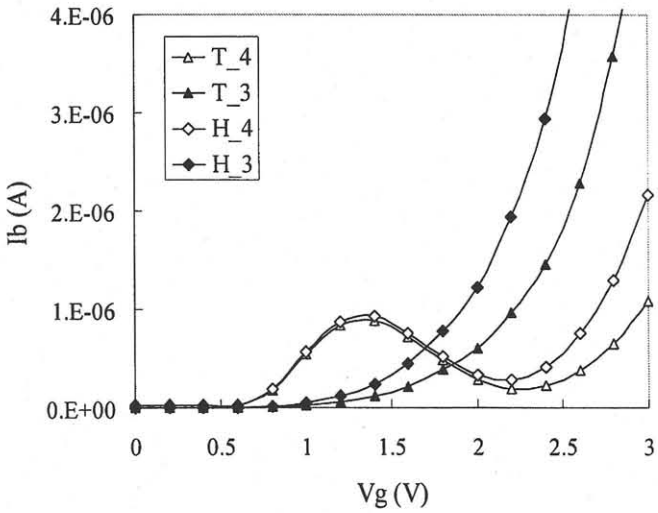

Fig. 6 Body current of H-gate is twice of T-gate due the parasitic tunneling effect, while the body currents due to impact ionization are identical.