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P9-11

An Efficient Unified Modeling of I-V Characteristics of SOI Transistors

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Abstract

In this paper, a new unified analytical I-V model for silicon-on-insulator (SOI) MOSFET is presented. The model is valid for possible transitions between partially-depleted (PD) and fully-depleted (FD) modes during the transistor operation. It is based on a non-pinned surface potential approach which is calculated accurately and efficiently in the model. Small geometry effects such as Channel Length Modulation (CLM), Drain Induced Barrier Lowering (DIBL), and high field mobility effects as well as self-heating effect are included in the formulation. The parasitic currents in each mode of operation is modeled with a proper formulation while a smoothing function is invoked for the transition between the operation modes. A comparison between the model and the experimental results shows good agreement over a wide range of drain-source and gate-source voltages.

1. Introduction

Devices fabricated in SOI technology have relatively thin body regions which are isolated from the Si substrate. During normal device operation, this region is either fully- or partially-depleted from majority carriers leading to FD and PD modes of operation. Some unified models have been published in the literature to present an I-V model valid for both modes of operation [1,2]. In the approach reported in [1], the mode of operation is not considered known as *a priori* and hence to calculate the drain current, first a numerical technique with an iterative procedure is employed to determine the mode of operation and, then, the front surface potential is calculated. This approach is computationally expensive for circuit simulation applications. In addition, the floating body effects used in this model, is more appropriate for PD devices. In the other unified model, first the critical gate voltage at which the transition between the operation modes occurs, is calculated and then the surface potential values for both PD and FD modes are calculated [2]. With the help of a smoothing function, a unified surface potential expression is presented. The front surface potentials obtained from the expression in the accumulation and strong inversion regions are considerably different from the numerical results. Additionally, parasitic BJT current formulation valid for FD mode of operation has been incorporated in the model. In this work, we present a new unified I-V model for PD/FD SOI which has higher efficiency and better accuracy compared to these previously reported unified models.

2. Operation Mode and Front Surface Potential

For a given film thickness, the operation mode of the SOI MOSFET changes by altering the bias voltage of the gate. To determine the operation mode of the device, similar to approach presented in [2], a critical gate voltage, V_{GFD}, is defined as

$$V_{GFD} = \frac{qN_{ch}t_{si}^{\,2}}{\varepsilon_s} + V_{Ff} - \frac{t_{si}}{\varepsilon_s}V_t C_d \exp\frac{V_{GFD} - (V_T - \Delta V_T) - \eta_f V_{cs}}{\eta_f V_t} \qquad (1)$$

where q is the electronic charge, N_{ch} is the substrate concentration, V_t is the thermal voltage, ε_s is the silicon permittivity of the silicon, V_{GF} is the front gate voltage, V_T is the threshold voltage, ΔV_T is the threshold voltage reduction due to longitudinal electric field, V_{Ff} is the front flat-band voltage, t_{si} is the SOI film thickness, C_d is the bulk depletion capacitance, η_f is the factor accounting for the reduction of the free channel charge due to the channel potential, and V_{cs} is the channel-source electron quasi-Fermi potential.

When V_{GF} is greater (less) than V_{GFD} the device operates in FD (PD) mode. Figs. 1 and 2 show the effect of film thickness and substrate doping on V_{GFD}.

The next step to calculate the drain current is to derive the front surface potential. Similar to approach presented in [1], the exact first integration of the 1D Poisson equation on the source side of the channel is used to obtain the surface potential. Here, the Poisson equation and the boundary conditions at the Si/SiO_2 interface are used to derive an implicit equation of both the front and back gate surface potentials, ψ_{sf} and ψ_{sb}, respectively. The relationship between these potentials, which is needed for solving the implicit equation, is given by

$$\psi_{sb} = \begin{cases} 0 & \text{in PD mode} \\ \psi_{sf} - qN_{ch}t_{si}^{\,2}/\varepsilon_s & \text{in FD mode} \end{cases} \qquad (2)$$

This leads to an implicit equation of ψ_{sf} which is solved using a second order Newton's method coupled with a good initial guess. Thus, the front gate surface potential can be calculated accurately and efficiently in the model.

3. Drain Current Model

Having a unified front surface potential, the IV characteristics of the device can be derived following the approach presented in [3]. The model is valid for both weak and strong inversion regions of device operation. The self-heating effect is also included based on the model of [4]. The floating body effects should also be included in the model. The formulations for the parasitic BJT is different in PD and FD modes of operation. This is due to the fact that in PD, a portion of the silicon layer is un-depleted while in FD the layer is totally depleted. In the previous unified models, either the PD model [1] or the FD model [2] has been used to include the parasitic BJT current. This approach may not be very accurate when the mode changes. In our proposed model, the parasitic BJT currents in PD [5] and FD [6] modes $I_{P,PD}$ and $I_{P,FD}$, respectively, are accurately calculated, and then the following smoothing function is utilized to present a unified model for the parasitic current I_P:

$$I_P = \frac{I_{P,FD}}{1+a\exp(\frac{V_{GF}-V_{GFD}}{bV_t})} + \frac{I_{P,PD}}{1+a\exp(-\frac{V_{GF}-V_{GFD}}{bV_t})} \quad (3)$$

Here a and b are fitting parameters.

4. Results and Conclusion

Figure 4, shows the simulation results of the proposed model for a device switching between the PD and FD modes. As it can be observed from the figure, a very good agreement exists between the drain current predicted by the model and the experimental results. This suggests that the proposed model can accurately model the I-V characteristics of the SOI transistor in both modes of operation.

References

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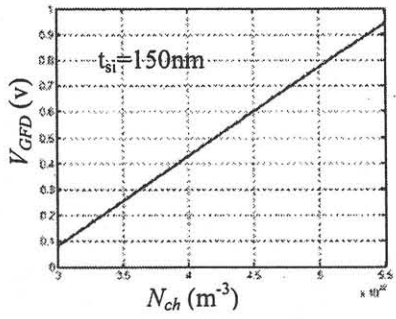

Fig. 1 Critical gate voltage as a function of substtrate doping

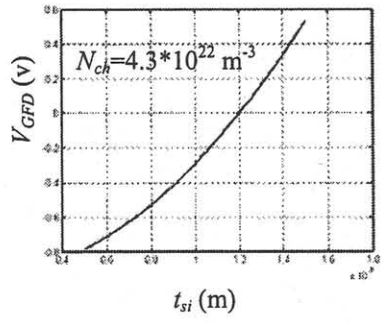

Fig. 2 Critical gate voltage as a function of film thickness

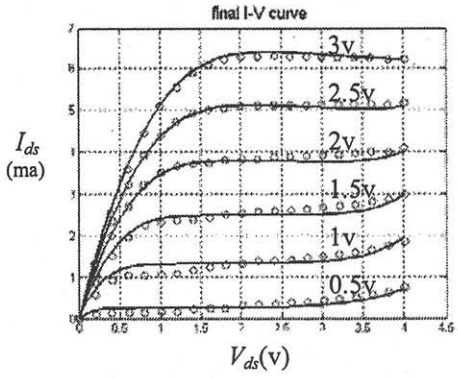

Fig. 3 Drain current characteristics for an SOI transistor with W=14 μm , L =0.7 μm , t_{si}=150 nm Solid lines are the model results and circles are experimental results of [1].