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No Defect Thermal Process for Thick SOI Bipolar Transistors with Trench Dielectric Isolations

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1. Introduction

Mixed signal bipolar CMOS DMOS (BCD) ICs using thick SOI wafers and trench dielectric-isolations (TD) have been widely used for automotive electronic control units for the advantages of the high-voltage high-density integration, high-immunity against electric surges and wide operating temperatures [1][2]. In the ICs, bipolar transistors are the key devices for the high-noise immunity and the high-packing density of linear circuits.

To deal with the two contradicting issues, the structure of the TD isolated bipolar transistor is attempted such that the base junction adjoins the isolation trench, as illustrated in Fig. 1. With this structure, the size of a transistor reduces by one seventh of that of a conventional junction isolation transistor having the same breakdown voltage of 120 V. However, the problem is the degradation of the transistor characteristics due to the crystal defects caused by the stress of the trench and local oxidation of silicon (LOCOS) [3].

This study copes with this issue by devising the novel stress-annealing thermal process so as to suppress the stresses and the crystal defects, which have been once formed after LOCOS in the area adjacent to the isolation trenches.

2. Experiments

Figure 1 shows a SOI bipolar transistor with TD, which has the breakdown voltages of 120 V and 35 V for the collector-base (BVcbo) and the collector-emitter (BVceo), respectively. The thickness of the SOI layer is 16 μm including a N^+ buried layer. The trenches are 3.0 μm in width and filled with the 600 nm thermal SiO2 on the each wall and the CVD poly silicon in the center. The top of the trench is oxidized by LOCOS process to the thickness of 980 nm after the surface planarization treatment of the trench. The base junction is 3.6 μm in depth and adjoins the trench. With this structure the minimum size of a bipolar transistor is reduced to 328 μm^2, one seventh of that of a conventional junction isolation transistor with the same breakdown voltage.

However, on the samples fabricated by the process flow shown in Fig. 2, some crystal defects were observed

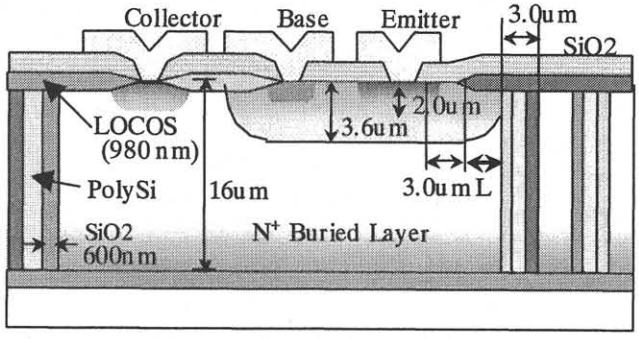

Fig. 1 Cross section of a SOI bipolar transistor with trench isolations.

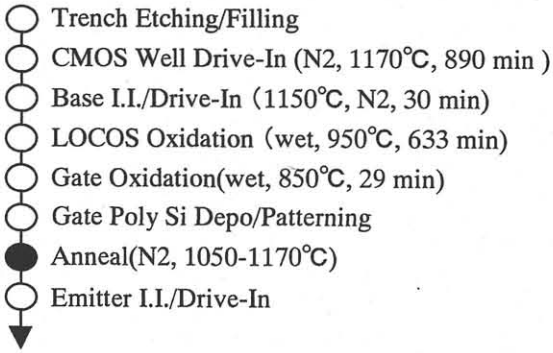

Fig. 2 Critical part of process flow for defect formation after trench

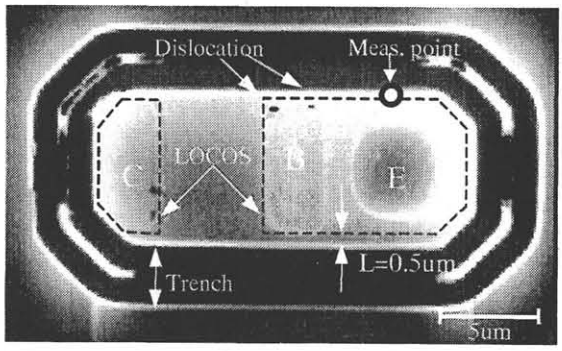

Fig. 3 Top view of the bipolar transistor showing the dislocation faults formed on the base area of the SOI bipolar transistor.

after the LOCOS oxidation in the base areas near the trenches, as illustrated in Fig. 3. On the assumption that the stresses of the trench and LOCOS caused them [4], it was investigated that weather a stress annealing thermal process inserted after LOCOS could cure the stresses and the crystal defects, by changing the temperature between 1050 ~1170°C.

3. Results and Discussions

Figure 4 shows the results of the defect-curing effects, evaluated for the h_{FE} distributions against the annealing temperature (Fig 4(a)) and trench-base distance, L (Fig. 4(b)) at a small collector current range of 1 μA, where they are sensitive to the defect densities.

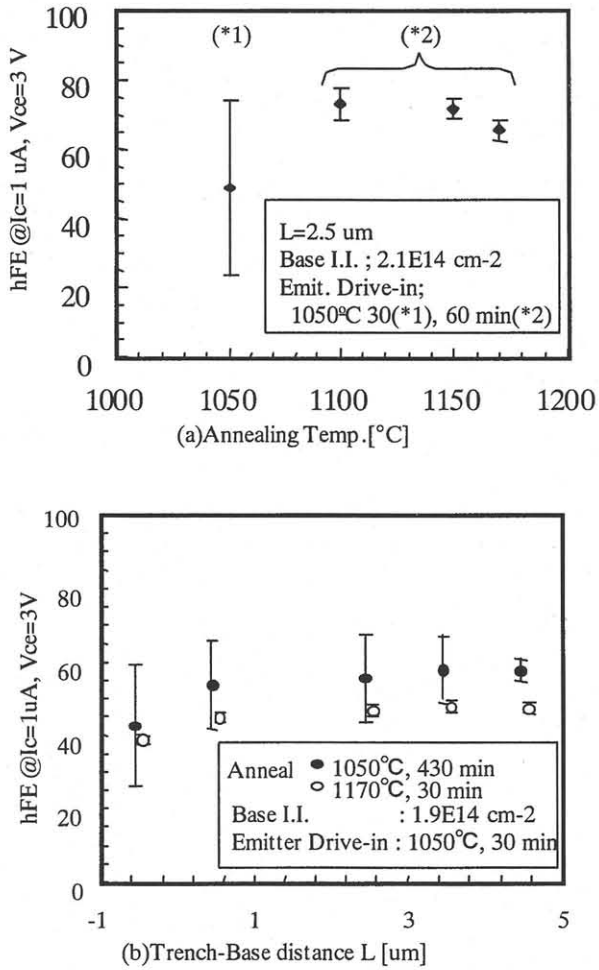

Fig. 4 h_{FE} vs. (a) annealing temperature and (b) trench-base distance.

From Fig. 4(a), the annealing temperatures above 1100°C decrease the h_{FE} distributions by about one sixth of that of 1050°C. Also from Fig. 4(b), for the samples annealed by 1170°C, the distributions are kept the same even when the trench and the base are overlapped.

To investigate the mechanism of the distinct improvements, the stress changes were measured by Raman shifts along the several process steps, at the same base surface spot, which was adjoining the trench and LOCOS as shown in Fig. 3. Figure 5 exhibits the results of the obvious stress relaxation by the annealing process.

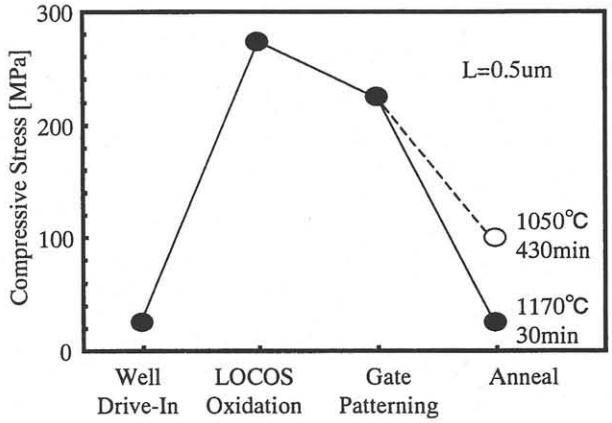

Fig. 5 Stress change vs. process flow of the base surface area measured by Raman shift.

Also, the samples before and after the annealing process were examined for the crystal defects by using Secco-etchant. As expected, while many defects were found on the samples before the treatment, they disappeared on the samples annealed with 1170°C.

From these facts, it is concluded that the inserted high-temperature annealing process not only relaxes the stresses associating with the trench-LOCOS structure, supposedly, due to the fluidizing of the oxides, but also cures the crystal defects, which once existed after the LOCOS process.

4. Conclusions

By inserting a high-temperature annealing process after the trench-LOCOS step, a no defect thermal process is devised for high-density SOI bipolar transistors.

References

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