High Performance p-channel SOI Schottky Barrier MOSFET Equivalent to p-n MOSFET

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1. Introduction

The Schottky barrier MOSFETs (SB-MOSFETs) are expected to overcome the difficulty in making the shallow junction. [1]-[2] However, the off-leakage current (IOFF) has been larger than p-n MOSFETs, because Schottky junction is more leaky than p-n junction. In the present work, the effect of the Schottky barriers (ϕ_{bn}) on device performance is studied by both simulations and experiments. It is found that high performance SB-MOSFET equivalent to p-n MOSFET can be fabricated by adjusting the barrier height and thinning width of gate sidewall, in addition to using silicon-on-insulator (SOI) substrates.

2. Simulations and Experiments

Simulations for SB-MOSFETs were carried out using ISE-TCAD Ver.6.1 simulator made by ISE Corp., Hydrodynamics model and both thermal and tunneling emission models for Schottky junction were assumed in device simulation. ϕ_{bn} is varied from 0.2 to 0.8 eV.

For experiments, SOI wafers with 100 nm-thick top Si layer (B-doped : 1.0×10^{15} cm⁻³) are used as substrates. Gate oxide thickness is 10 nm, and the gate length and width are 10 μ m and 3 μ m, respectively. Three-types of device structure shown in Fig. 1 are investigated. The first type is the SB-MOSFET having Schottky junctions at both source and drain, the second has a Schottky junction at only source or drain, and the third is the conventional p-n MOSFETs. Additionally, three types of silicide are used for source and drain, ErSi17, NiSi and PtSi, to know the effect of difference of ϕ_{bn} . 4.0 × 10¹⁵ cm⁻² of Boron difloride (BF₂) and phosphorus (P) were implanted to source and drain, and activated at 850℃ for p and n-channel p-n MOSFETs, respectively.

3. Results and Discussion

For the SB-MOSFET, drain current is strongly related to ϕ_{bn} . Figure 2 shows simulated results for the relation of ϕ_{bn} and I_{ON} , i.e., hole current from source or I_{OFF} , i.e., electron current from drain for p-channel operation at $V_d = -$ 0.3 V. As shown in Fig. 2, as ϕ_{bn} , increases, I_{ON} is increased and IOFF is decreased. This is explained by that as barrier height for p-Si (ϕ_{bp}) decreases, hole current crossing over the barrier or tunneling through the barrier is increased.

Contrary to it, as ϕ_{bn} decreases, the I_{OFF} from drain is increased. The similar story can be mentioned for n-channel operation. Figure 3 shows the experimental results for SB-MOSFETs with Schottky junction at source and p-n junction at drain. The p-n junction at drain blocks the electron leakage current from drain and makes it easier to observe hole current from source. Here, the measurements were carried out for the three types of ϕ_{bn} . I_{ON} increases as ϕ_{bn} increases. The experimental result demonstrates the validity of the simulated results.

In p-channel SB-MOSFETs, total currents are expressed as the summation of hole current from source and electron current from drain. Figure 4 shows the experimental results for the relation of the barrier height and ION or IOFF for pchannel operation at $V_d = -1.5$ V for the Schottky MOSFET. I_{ON} and I_{OFF} reflect the barrier height as mentioned in Fig 2. When ϕ_{bn} is high, I_{ON} is increased for p-channel. The same can be said for n-channel SB-MOSFETs. From simulated results, over 8-orderd ratio of ON/OFF current at $V_d = \pm$ 0.3 V is obtained in case of ϕ_{bn} less than 0.3 eV of ϕ_{bn} for n-channel operation and less than 0.8eV for p-channel operation.

To obtain higher ION in SB-MOSFETs, the width of sidewall is decreased. Figure 5 shows the simulated results for the relationship between drain current and width of the sidewall. Drain currents increase in double when the width changes from 122 nm to 23 nm. It is due to the parasitic resistance at spacer region. Formation of sidewall by thermal oxidation can make the width of thin sidewall precise and it was carried out in wet oxygen at 850°C to obtain 20 nm-wide sidewall.

Figure 6 shows the comparison of characteristics for the fabricated PtSi SB-MOSFET and p-channel p-n MOSFET at $V_d = -0.3 V$ and -3.3 V. I_{ON} and I_{OFF} of the PtSi SB-MOSFET are almost equal to those of p-n MOSFET and the I_{ON} is slightly larger than the prediction by simulation. Figure 7 shows output characteristics for both PtSi SB-MOSFETs at 125 and 300 K. Little difference of ION is observed for PtSi SB-MOSFETs as like p-n MOSFETs. The phenomenon was not observed for NiSi and ErSi SB-MOSFETs. PtSi Schottky junction at source is considered to have ϕ_{hn} much less than 0.26 eV of theoretical value. Here, it was summarized that the PtSi SB-MOSFET can realize ION and

 l_{OFF} as much as p-n MOSFET by selecting proper material with low barrier height for source.

4. Conclusions

It is found that high performance SB-MOSFET equivalent to p-n MOSFET can be fabricated by adjusting the barrier height and thinning width of gate sidewall, in







Fig. 2. Simulated results for the relation of ϕ_{bn} and I_{ON} or I_{OFF} for p-channel operation at $V_d = -0.3 V$.



Fig. 3. Experimental results for SB-MOSFETs with Schottky junction at source and p-n junction at drain at $V_d = -1.5 \text{ V}$.



Fig. 4. Experimental results for SB-MOSFETs with Schottky junction at source and drain at $V_d = -1.5 V$.

addition to using SOI substrates.

References

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- [2] W. Saitoh, S. Yamaguchi, A. Itoh and M. Asada, Jpn. J. Appl. Phys. 38, L629 (1999).



Fig. 5. Simulated results for the relationship between the drain current and the width of the sidewall at $V_d = -3.3$ V.





(b) Transfer characteristics $(V_d = -3.3 V)$

Fig. 6. Comparison of characteristics for PtSi SB-MOSFET and p-channel p-n MOSFET.



Fig. 7. Output characteristics for both PtSi SB-MOSFETs at 125K and 300 K.