Abstract — In this paper, we show that with a positive body bias, the electrical characteristics of MOSFETs can be improved for those applications which are primarily concerned with threshold matching effect. The positive body bias is then applied to improve the short channel effect and to reduce the active power. Making the body available improves the devices and enables new applications. We present the matching characteristics with partially depleted SOI NMOSFETs.

I. INTRODUCTION

Low-power/high-speed SOI-RF device and circuit become more important components for wireless communication equipment. The mainstream of RF applications is usually implemented in GaAs or silicon bipolar technology. Advances in CMOS process technology have continued to reduce the minimum channel length of MOSFETs, thereby increasing the cut-off frequency \( f_T \) of the devices \([1]-[4]\). Because of these relatively high \( f_T \) values, CMOS device technology is becoming a viable choice in analog and RF applications for portable wireless communication systems that need the low power and high speed. However, the parasitic capacitances of bulk-silicon MOSFETs (such as S/D junction to well capacitance and well junction to substrate capacitance) have a strong influence on the achievable quality factor and often form undesirable coupling paths, which reduce the achievable isolation between different circuit nodes. SOI CMOS has a reduced parasitic junction capacitance and is in perfect isolation by BOX and STI. PD-SOI device has the independent neutral body region, so we can apply independently body bias without additional process steps. Although much work has been done on both analog and digital performances of the SOI \([5],[6]\) and bulk-silicon devices \([4],[7]-[11]\), the effects of body bias and \( V_{DS} \) matching on the analog performance of PD- SOI CMOS devices have not been reported extensively in literature.

II. DEVICE STRUCTURE

The starting 8" SIMOX wafer has the silicon film thickness of 100 nm and buried oxide thickness of 100 nm. 0.18 \( \mu \)m dual poly (n+p+) gate PD-SOI process is applied to fabricate devices with 3.8 nm-gate oxide. Key process steps are STI, boron (arsenic) for LDD and S/D of PMOSFETs (NMOSFETs) RTA (1000 °C, 25 s) and salicide process for reducing gate and S/D sheet resistance. The threshold voltage adjustment ion doses were determined to have \( V_{TH} \) of 0.35 V for NMOSFETs and -0.35 V for PMOSFETs.

III. ELECTRICAL CHARACTERISTICS

Fig. 1 shows the cross sectional view of the three different body structures, such as conventional triple well, modified triple well, and SOI structures. In Fig. 2, the threshold voltage roll-off versus channel length are compared for various \( V_{DS} \) conditions (\(-0.5, 0, 0.25, +0.25, +0.5 \) V and floating body). The forward biased \( V_{TH} \) difference (\(+0.25-\) and \(+0.5 \) V) between minimum channel length and \( L_g \) of 1 \( \mu \)m are smaller than those of others (\(-0.5, 0, \) floating body). Because of decreased charge sharing effect due to narrowed depletion region, short channel effect is improved with increasing \( V_{TH} \). For example, \( L_g \) with \( V_{DS} \) of \(-0.5 \) V has a margin of about \( 0.05 \mu \)m over that with \( V_{DS} \) of \(-0.25 \) V. The matching effects are important design parameters in precision analog circuit applications such as data converter and switched-capacitor filter. The effect in SOI devices is investigated considering scaling in device dimensions and supply voltage. Difference \( \Delta V_{TH} \) between a pair of MOSFETs is usually described by the standard deviation of \( V_{TH} \) \([6],[7],[10],[11]\):

\[
\Delta V_{TH} = \sqrt{\frac{q}{g_m}} \frac{2N_a}{N_{S/D}} \frac{V_F}{L_{W/L}}^{1/2}
\]

(eq-1), where \( g_m \), \( W \), \( L \), \( N_a \), \( N_{S/D} \), and \( q \) are the gate oxide thickness, the device width, the channel length, the depletion width, the doping concentration of body, and the permittivity of silicon, respectively. This equation is based on the assumption that mismatch is caused by independent random disturbance of physical properties and that the correlation distance of the statistical disturbance is small compared to the active area \([7],[10],[11]\). Figs. 3(a) and (b) are the measured \( \sigma V_{TH} \) values as a function of inverse square root of the channel area \((W \times L)\) with various \( V_{DS} \) values (-0.25, 0, +0.25 and +0.5 V) as the parameter and derived matching coefficient, respectively. \( \Delta V_{TH} \) decreases due to the reduction of depletion layer width as the body potential increases from negative to positive bias. The overall dependence of \( \Delta V_{TH} \) with the body bias condition is proportional to \( V_{DS}^{0.25} \), showing that \( \Delta V_{TH} \) can be reduced by applying forward \( V_{DS} \) bias independently to the SOI devices. Fig. 3(a) demonstrates that the devices with dimension near the lithographical limit of the feature (small area device such as \( W/L = 0.18 \), 0.25 and 0.625) result in drastically increased standard deviations in \( V_{TH} \), which can be reduced by the positive body bias. On the other hand, (2) \([12]\) can be derived to include the effect of the depletion width of drain to body as:

\[
\sigma V_{TH} = \sqrt{\frac{q}{g_m}} \frac{2N_a}{N_{S/D}} \frac{V_F}{L_{W/L}}^{1/2}
\]

(eq-2), where \( W_m \) is the average of depletion width for the pin junction of drain \( n^+ \) region. This equation is based on the assumption that doping concentration and \( W_m \) are independent of the gate length. The \( \Delta V_{TH} \) from (2) is calculated to be lower than 1 mV (\( W/L = 0.25 \)) and 0.4 mV (\( W/L = 0.18 \)), which are much lower than the measured values. It can be argued that the major reason for the \( V_{TH} \) variation is the variation of gate length and doping concentration in the short channel devices. However, the calculated \( V_{TH} \) increases (from 1 mV to 7 mV) as channel width decreases (from 20 \( \mu \)m to 0.25 \( \mu \)m at 0.2 \( \mu \)m of \( L_g \)). It means that small size devices (narrow width and short channel device) are more effective than large devices in applying forward body bias. In order to see the effect, the change of site variation of \( V_{TH} \) according to \( V_{DS} \) conditions (\(-0.25, 0, +0.25 \) and +0.5 V) are shown in Fig. 4 for three different \( L_g \)'s (0.2, 0.25 and 0.7 \( \mu \)m). For a positive \( V_{DS} \), we obviously observe small site variation and standard deviation of \( V_{TH} \) due to the improvement in short channel effect as the depletion width decreases [Fig. 4(a)]. The matching effect (Arv) and \( V_{TH} \) site variation effect are improved for the positive \( V_{DS} \) over the data under zero or negative \( V_{DS} \) condition. Hence, the positive \( V_{DS} \) of the NMOSFETs would lead to the observed lower \( V_{TH} \) values for matching coefficient \( A_r \). In the device scaling with same technology level, it is very effective to apply the positive body bias to improve the matching characteristics because the depletion width \( (x_d) \) reduces with \( V_{DS} \). Fig. 5 shows the threshold voltage slope variation \(
\Delta V_{TH} = \sqrt{\frac{q}{g_m}} \frac{2N_a}{N_{S/D}} \frac{V_F}{L_{W/L}}^{1/2}
\)

(eq-2) with PD-SO|, PMOS \( \Delta V_{TH} \) (\(-0.5 \) V) is show.

IV. CONCLUSION

It has been shown from various measurements that the positively biased body voltagecould improve the circuit performance of SOI technology. Especially, the method to design the analog and RF circuits with the consideration of body bias effect has been proposed.

ACKNOWLEDGEMENT

This work is supported by Brain Korea 21 Project (BK21) and by the National Research Laboratory Project of the Ministry of Science and Technology (NRL).

REFERENCES

Fig. 1. Cross-sectional view of three different device structures where (a) conventional triple well in bulk Si, (b) modified triple well in bulk Si, and (c) SOI MOSFETs.

Fig. 2. Short channel effects with various body bias conditions. SCE improves as $V_b$ increases to forward bias.

Fig. 3. (a) $\sigma V_{TH}$ of NMOSFETs versus the inverse square root of the area, for sub-0.2 $\mu$m technology, (b) Comparison of measured $\sigma V_{TH}$ and calculated $\sigma V_{TH}$ (drain depleton effect) (c) Matching coefficient, $A_{VT}$, for PD-SOI NMOSFETs in various body bias. The coefficient is calculated from (1).

Fig. 4. Threshold variation effects by body bias as follows: (a), (b) and (c) are the variation of threshold voltage at various channel length ($L_C = 0.2$ $\mu$m, 0.25 $\mu$m, and 0.7 $\mu$m) and body bias ($V_b = -0.25$ V, 0V, +0.25 V and +0.5 V).

Fig. 5. Comparison of threshold voltage slope characteristics where (a) $V_{TH}$ ($V_b = -0.25$ V, +0.25 V and +0.5 V) vs. $V_{TH}$ ($V_b = 0$V), (b) Slope change caused by body bias, and (c) correlation of threshold voltage with 0.7 $\mu$m of $L_C$. 

591