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A Novel Diffusion Capacitance Characterization Technique for the Parasitic BJT in PD SOI MOSFET's

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1. Abstract

A novel diffusion capacitance characterization technique of the injected minority carriers has been developed for the parasitic bipolar transistor (BJT) in partially depleted (PD) SOI MOSFET's. This technique was experimented for a pn-junction diode, which was fabricated in 0.3um CMOS process, and applied for the parasitic BJT, which was fabricated in 0.3 um PD SOI process.

2. Introduction

The characterization of a parasitic BJT is very important for PD SOI MOSFET's because the increased body potential activates the BJTs, which produces significant bipolar current. The diffusion capacitance measurement of the injected minority carriers is the most difficult in the parasitic bipolar characterization since the forward capacitance measurements using Impedance analyzers cannot be applied for the purpose [1]. Even though the two-frequency capacitance measurement technique [2] was used, it would be failed in the strong forward bias region because of the measured negative capacitances. We have developed a novel diffusion capacitance characterization technique for strong forward voltage, which is obtained by solving the relation between a small-signal equivalent circuit model of the parasitic BJT including body resistances and two measured S-parameter sets at each forward bias.

3. Theory and Experimental Results

The forward diffusion capacitance measurement technique due to this work was experimented for the pn-junction diode and the parasitic BJT in PD SOI MOSFET's. In order to obtain the accurate capacitance characteristics, the effect of probe pads and the metal interconnections has been de-embedded from the measured S-parameters by using the three-step de-embedding method [3]. The small-signal equivalent circuit models of these devices are shown in Fig. 1 and 2. Here, C_i represents the intrinsic capacitance, G_i is the intrinsic conductance, and R_s is the series resistance. We solve the relations between small-signal equivalent circuit and the total reactance at two frequencies for the intrinsic capacitance C_i. The intrinsic capacitance is obtained as:

$$C_i = \frac{\omega_a \cdot X_b - \omega_b \cdot X_a}{X_a \cdot X_b \left(\omega_b^2 - \omega_a^2\right)} \quad (1)$$

$$X_{a,b} = imag\left(\frac{\left(1+S_{11a,b}\right)\left(1+S_{22a,b}\right) - S_{12a,b}S_{21a,b}}{2Z_c S_{12a,b}}\right) \quad (2)$$

where, ω_a and ω_b are the measured angular frequencies, X_a and X_b are measured reactance, $[S]_a$ and $[S]_b$ are the measured S-parameters, and Z_c is the system impedance. The series resistance and intrinsic conductance value do not need to be accurate. The only requirement is that the equivalent circuit needs to be independent of the measured frequency. Fig. 3 is capacitance versus voltage (CV) characteristics of the pn-junction diode to validate the proposed technique. Fig. 4 shows the CV characteristics of the parasitic BJT in PD SOI nMOSFET's using the proposed technique.

References

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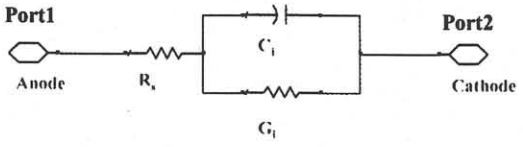

Fig. 1. A small-signal equivalent circuit model of a pn-junction diode.

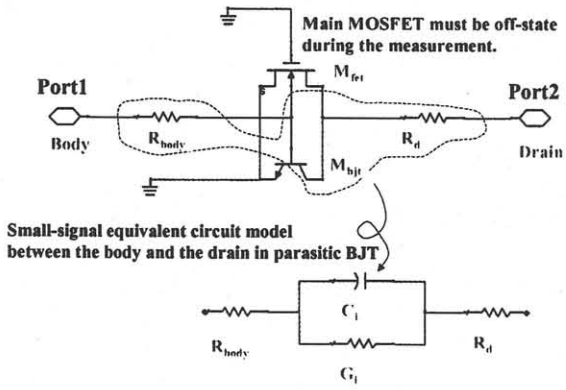

Fig. 2. A PD SOI nMOSFET with a small-signal equivalent circuit model between the body and the drain in a parasitic npn BJT. Here, M_{fet} represents the main SOI nMOSFET, M_{bjt} is the parasitic npn BJT, R_{body} is the body resistance, and R_d is the drain resistance. R_s is the sum of body resistance and drain resistance. Main nMOSFET should be off-state (V_g=V_s=0V) during the S-parameter measurements since we have to merely characterize the parasitic BJT.

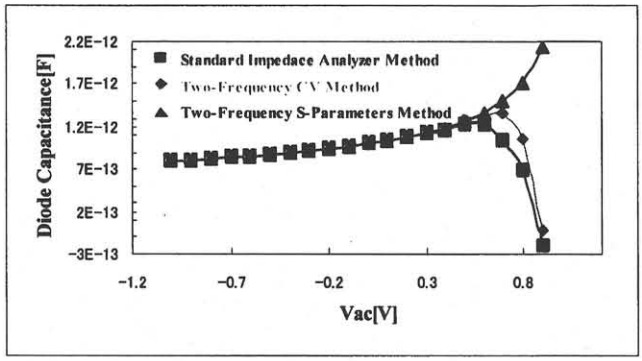

Fig. 3. CV characteristics of a junction diode using the three methods. Here, the frequencies to be measured for two-frequency CV method are 600KHz and 1MHz. The frequencies to be used for two-frequency S-parameters method are 500MHz and 1GHz. In the reverse and the weak forward bias regions, all three methods represented almost the same and accurate value. However, the standard Impedance Analyzer and the two-frequency CV methods do not work in the strong forward bias region, and results show negative capacitance. Since the intrinsic conductance G_d has been significantly increased, dc current flows into the Impedance Analyzer and the effect of series resistance R_s cannot be negligible. By contrast, the result of two-frequency *S*-parameters method with the proposed technique shows the theoretical curve even in the strong forward bias region.

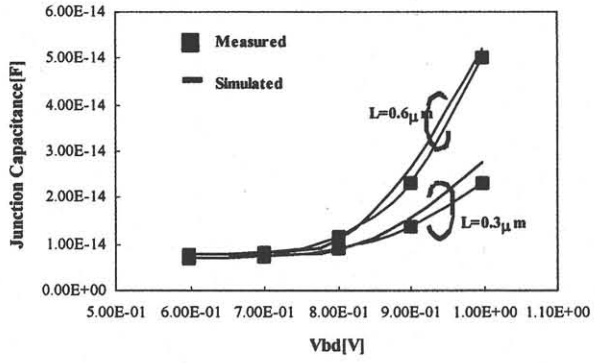

Fig. 4. Characteristics of the junction capacitances between body and drain in the parasitic BJT. Here, measured data is obtained by using proposed two-frequency *S*-parameters method and simulated data is obtained by simulating BSIMPD SOI 2.2 model of University of California, Berkeley. Transit time parameters have been extracted from the measured forward diffusion capacitances. Other DC and CV parameters have been accurately extracted in advance. We adopted two different gate channel length (L=0.3μm, 0.6μm) SOI devices as shown in the figure. The gate channel width of these two is 20 μm.