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RF Power Characteristics of Thin Film Silicon-on-Sapphire MOSFET

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Introduction

Thin film Silicon-on-sapphire (SOS) MOSFETs are promising devices for RF applications owing to the favorable characteristics including reduced parasitic resistance, better short channel immunity, reduced cross-talk and minimal capacitive substrate loss. While most of the research on SOS MOSFETs have concentrated on small-signal RF characterization (via S-parameter and RF noise measurement) and RF circuit applications such as LNA, mixer and VCO [1], the RF power applications using SOS MOSFETs have seen far less reported results [2], partly due to the limited breakdown voltages in SOS MOSFETs that limit the power delivering capability. On the other hand, the fast developing short-range, low- or medium-power applications such as bluetooth and wireless LAN results in our renewed interests in SOS MOSFET RF power amplfiers. A recent report [3] on the power amplifier characteristics revealed the promising RF power performance of SOS MOSFET, even though the characteristics were obtained with both input and output terminated with 50 Ohm - unmatched. However, for the optimum design of RF power amplifiers, large-signal load-pull measurement, which reveals the impedance matching information, is essential. In this paper, we report the first detailed large-signal load-pull characteristics of SOS MOSFET at 2 GHz. A Maury MT982B01 load-pull system with automatic impedance tuners was used to match the device to achieve maximum output power (P_{out}), gain (G) and power added efficiency (PAE). To characterize the linearity of the power transistors, third order intermodulation (IM3) and adjacent channel power ratio (ACPR) were also measured using the same load-pull system.

Device Characterization

The device used in this work was fabricated using a commercial 0.5-μm SOS CMOS process. The SOS MOSFET has a nominal gate width of 972 μm. DC current-voltage (I-V) characteristics are shown in Fig. 1 and Fig. 2. The device exhibits a threshold voltage of 0.1 V and an off-state breakdown voltage of 3.2 V. At V_{DS} = 3.0 V, a maximum drain current density of 330 mA/mm and a peak transconductance of 100 mS/mm are achieved. On-wafer S-parameter measurement using Agilent 8722E network analyzer and Cascade microwave probe shows cutoff frequency f_t (current gain cutoff frequency) and f_{max} (unilateral power gain cutoff frequency) of 13.8 GHz and 41 GHz, respectively, as shown in Figure 3.

On-wafer load-pull measurement was performed using Maury's automated tuning system and Agilent E4419B power meter. Conjugate matching was used for the source (gate), and the load impedance was tuned to achieve maximum Pout and PAE, respectively. The gate bias V_{GS} was set at 0.5 V so that the power SOS MOSFET operated in class AB to achieve high Pout and PAE. The drain bias was varied from 1.5 to 3.0 V, for search of optimum operating point. When the load was matched to maximize the Pout, an Pout of 12.5 dBm along with a gain of 18 dB were obtained at V_{DS} = 2.5 V and V_{GS} =0.5 V, as shown in Fig. 4. When the load was matched to maximize the PAE, an optimum PAE of 55% was observed, as shown in Fig. 5, with the same bias voltages. The high PAE compares favorably with that reported results for another type of silicon-based RF power transistors: SOI lateral-diffused MOS transistor (LDMOS) [4].

The recent employment of wireless communication standards, such as IEEE 802.11a, CDMA and W-CDMA is imposing more demanding requirement on the linearity of the RF power amplifiers. To characterize the linearity of the power SOS MOSFET, we carried out third order intermodulation measurement with two-tone signals (with a frequency separation of 50 MHz) at 2 GHz. The load was once again matched to maximize Pout. Fundamental, IM3 are shown in Fig. 6. This yields an third order intermodulation intercept (IP3) of 18 dBm (output power). Using a W-CDMA modulated signal source with a bandwidth of 50 KHz, ACPR for adjacent and alternative channel was measured and shown in Table 1. A comparison with CMOS and LDMOS in the linearity will be provided.

Conclusion

Detailed large-signal load-pull characteristis are presented for the first time for thin film SOS MOSFET RF power thin film SOS MOSFET. Power-added efficiency as high as 55% was achieved. Linearity characterization is also presented.

Acknowledgements

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References

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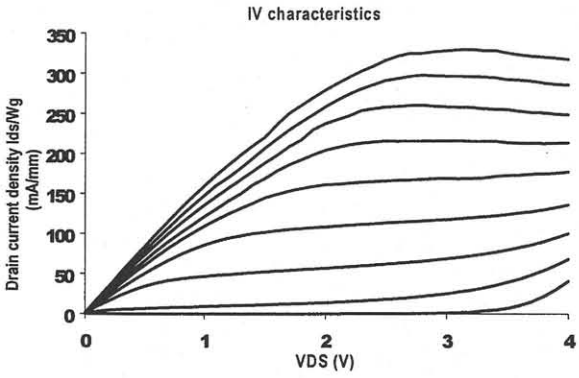

Fig. 1: DC current-voltage characteristics of low threshold SOS MOSFET V_{GS} = 0-4V; 0.5V step

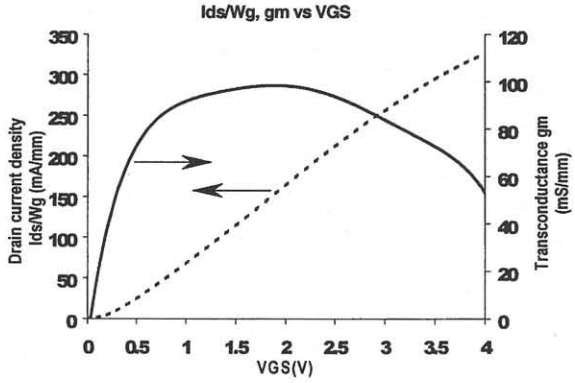

Fig. 2: I_{DS}/W_g, gm vs V_{GS} at V_{DS}=3V

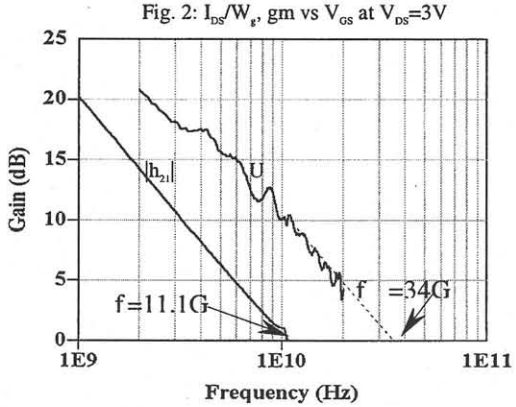

Fig. 3: f_t and f_{max} at V_{GS}=2V, V_{DS}=3V

Pin=0dBm	Pout (dBm)		ACPR (dBc)			
			Adjacent Channel		Alternate Channel	
	50ohm	Max Pout	50ohm	Max Pout	50ohm	Max Pout
VGS=0.5V VDS=1.5V	6.85	7.03	-35.37	-25.86	-61.37	-46.58
VGS=0.5V VDS=2V	6.37	9.55	-36.56	-28.31	-63.84	-49.17
VGS=0.5V VDS=2.5V	7.31	11.46	-39.23	-27.95	-64.50	-50.55
VGS=0.5V VDS=3V	8.45	12.55	-39.03	-23.27	-63.77	-44.61

Table 1: ACPR comparison between mismatched and matched impedance

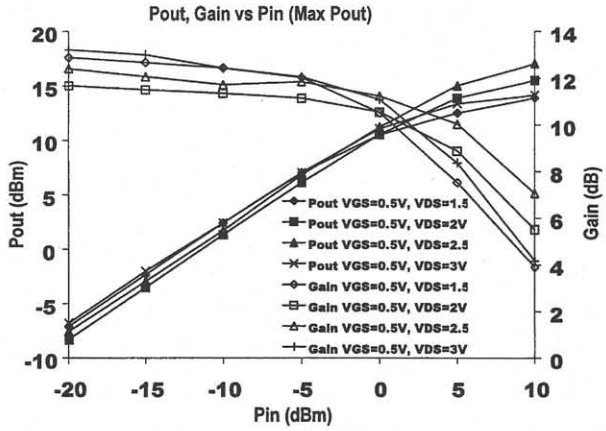

Fig. 4: Input-output power characteristics of SOS MOSFET at various biasing conditions

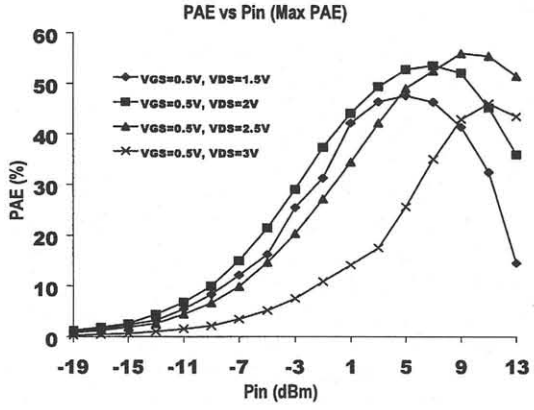

Fig. 5: PAE versus input power at different biasing conditions

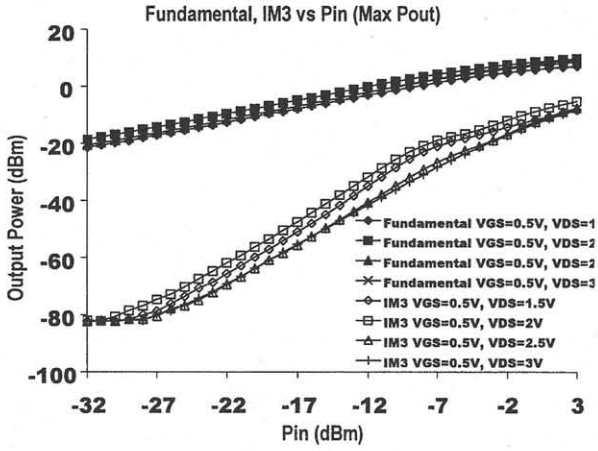

Fig. 6: Output power of fundamental and IM3 vs input power at different biasing conditions