

**'History Effect'-Free Operation of 'SBB' SOI MOSFETs**

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3-4-1 Ozuka-higashi, Asaminami-ku, Hiroshima, 731-3194, JAPAN E-mail: terauchi@ieee.org**Abstract**

Transient characteristics of 'Self-Body-Biased' ('SBB') SOI MOSFETs [1,2] have been studied in detail. Simulation results reveal that there is no history effect in propagation delay in 'SBB' SOI inverters whereas strong history effect exists in conventional floating-body counterparts. This is because 'SBB' SOI MOSFETs in their 'OFF' state are functionally equivalent to body-tied partially-depleted SOI MOSFETs, allowing excess majority carriers, which are the main cause for the 'history effect,' to be swept away from the body terminal every time they go to their 'OFF' state..

**Introduction**

'SBB' SOI MOSFETs [1,2] have been introduced to overcome the inapplicability of dynamic threshold MOSFETs [3] to the conditions requiring operating voltage higher than 0.6 volt (V). In order to enhance their current drivability 'SBB' SOI MOSFETs utilize body potential modulation by the generated majority carriers [1], resulting smaller inverter propagation delay than that in conventional body-tied partially-depleted SOI inverters [2]. Former works did not mention whether there is 'history effect' [4] in their operation. Although it is reported that the 'history effect' in SOI devices has only limited impact on circuit performance [5], it inevitably requires much more careful and precise treatment in SOI circuit design, making SOI circuit design by far difficult and expensive. Therefore the 'history effect' should be eliminated if possible.

In this paper the authors present a detailed analysis as to transient change in body potential of 'SBB' SOI MOSFETs as well as that in floating-body counterparts. It has been revealed that, although they utilize the accumulated majority carriers, there is no history effect in propagation delay in 'SBB' SOI inverters.

**Simulation Methodology**

Figure 1 illustrates (a) the basic concept and (b) the '2D device structure' of an 'SBB' SOI MOSFET. In order to simulate the characteristics of the inherently three-dimensional 'SBB' devices by only using a 2D-device simulator (Medici, available from Avant! Corp.) the authors have also utilized the modified double gate device structure (Fig.1 (b)) [1]. Both gate voltages were kept the same. Device parameters used in this study are summarized in Table 1. Body potential was measured at the SOI-BOX interface (point X) beneath the center of the main gate electrode.

**Results and Discussion**

Figure 2 shows transient change in body potential both in the n-channel device in an 'SBB' SOI inverter and in the one in a floating-body SOI inverter as well as their output waveforms. Body potential in the n-channel device in an 'SBB' SOI inverter recovers its initial value after input voltage ( $V_g$ ) becomes 0 V (20 ns ~ 40 ns) whereas that for a floating-body SOI inverter becomes by about 0.4 V higher than its initial value. This positive

increase in body voltage explains faster transient response in a floating-body SOI inverter than that in an 'SBB' counterpart (shown in top of Fig.2). Fast recovery in body potential in an 'SBB' SOI inverter after  $V_g$  becomes 2 V (0 ns, 40 ns) indicates that the body potential modulation in 'SBB' SOI MOSFETs lasts primarily during the period when the carrier generation by impact ionization occurs. This is because the 'excess' part of majority carriers can be drawn out through the potential valley beneath the auxiliary gate electrode over the 'low Na' region even in its 'ON' state. In floating-body devices the body potential modulation is by far prolonged because there is no apparent 'sink' for the majority carriers (they must go beyond built-in potential barrier).

Figure 3 and 4 show body potential changes for different pulse width in the n-channel device in an 'SBB' SOI inverter and in the one in a floating-body SOI inverter, respectively. Figure 3 clearly indicates that there is no history effect in an 'SBB' SOI inverter. This is because 'SBB' SOI MOSFETs in their 'OFF' state are functionally equivalent to body-tied partially-depleted SOI MOSFETs, enabling excess majority carriers, which are the main cause for the 'history effect,' to be swept away from the body terminal every time their inversion channel disappears. On the other hand the existence of strong history effect in a conventional floating-body SOI inverter is apparent (Fig.4). Thus much more robust operation can be expected for circuits utilizing 'SBB' SOI MOSFETs than for those using floating-body counterparts. In addition circuits utilizing 'SBB' SOI MOSFETs are expected to work much faster than those using body-tied SOI MOSFETs do [2].

It should be noted that the increased terminal capacitance due to the reduced depletion layer width in 'SBB' SOI MOSFETs (Fig.5) may cause circuit performance degradation to some extent, especially in the case with light load. The reduced depletion layer width is realized through the body potential modulation, and is inherent to the 'SBB' MOSFET operation. The increased drain capacitance when  $V_d = 2$  V and  $V_g = 1$  V in an 'SBB' SOI MOSFET as compared with that in a body-tied SOI MOSFET, partly explains the operating voltage dependence of  $\tau_{pd}$  improvement in an 'SBB' inverter [2], where performance improvement in 'SBB' inverters becomes less dominant as operating voltage becomes higher than 1.2 volt.

**References**

- [1] M.Terauchi and K.Terada, Proc. 1999 IEEE International SOI Conference, p.36.
- [2] S.Funakoshi, M.Terauchi, and K.Terada, Proc. 2000 IEEE International SOI Conference, p.52.
- [3] F.Assaderaghi, D.Sinitsky, S.Parke, J.Bokor, P.K.Ko, and C.Hu, Technical Digest of IEDM'94, p.809.
- [4] D.Suh and J.G.Fossum, Technical Digest of IEDM'94, p.661.
- [5] F.Assaderaghi and G.Shahidi, Proc. 2000 IEEE International SOI Conference, p.6.

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|------------------------|--------------------------|---|
| $L_g=0.25 \mu\text{m}$ | $T_{ox}=5 \text{ nm}$    | $\text{high Na}=2.0 \times 10^{17} \text{ cm}^{-3}$ |
| $W_n=1.0 \mu\text{m}$  | $T_{soi}=100 \text{ nm}$ | $\text{low Na}=6.0 \times 10^{16} \text{ cm}^{-3}$  |
| $W_p=2.0 \mu\text{m}$  | $T_{box}=100 \text{ nm}$ | $C_L=1.0 \text{ pF}$                                |

Table 1 Device Parameters

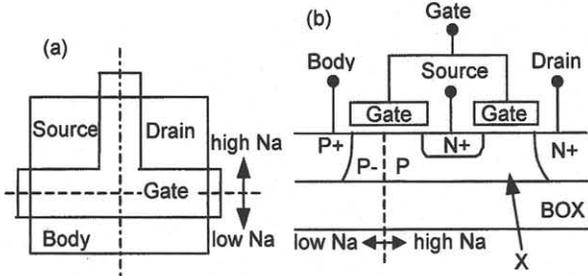


Fig. 1 (a) Basic concept (the plan view) and (b) '2D device structure' of an 'SBB' SOI MOSFET.

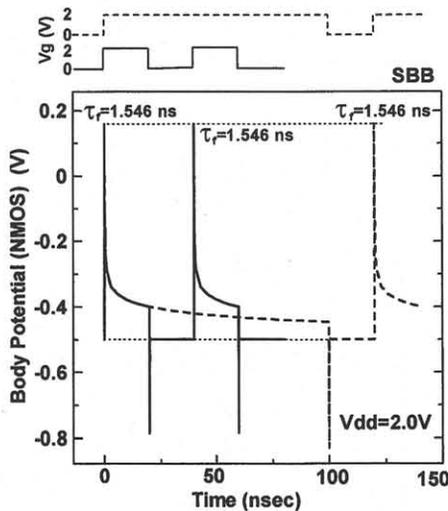


Fig. 3 Pulse width dependence of body potential change and fall-time variation in an n-channel 'SBB' SOI MOSFET.

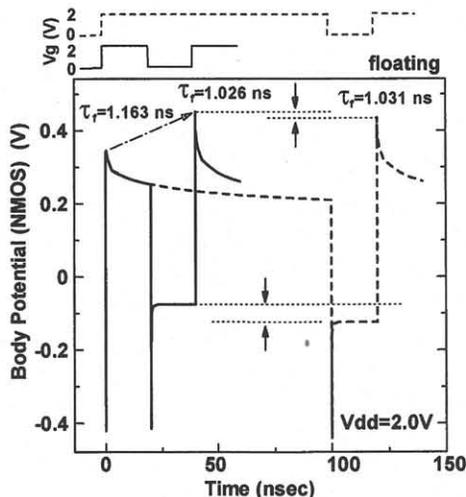


Fig. 4 Pulse width dependence of body potential change and fall-time variation in an n-channel floating-body SOI MOSFET.

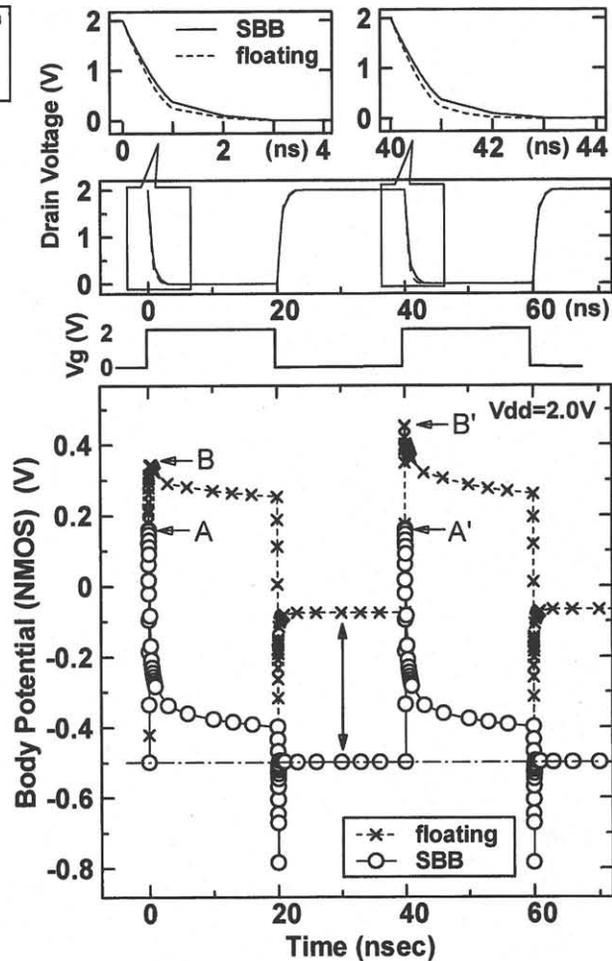


Fig. 2 Transient response in an 'SBB' and a floating-body SOI n-channel MOSFET.

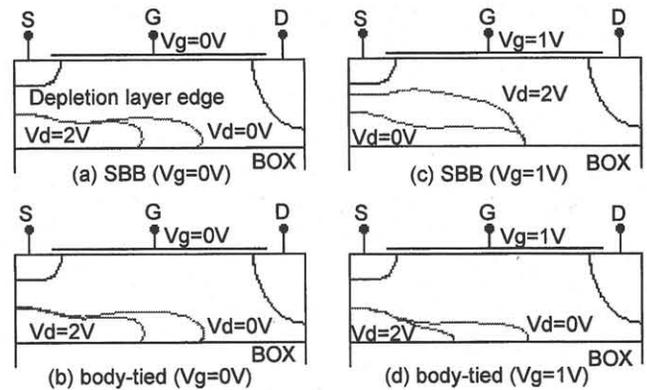


Fig. 5 Bias voltage dependence of the depletion layer width in an 'SBB' and a floating-body SOI n-channel MOSFET.