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SOI MOSFET with Body-Terminal-Controlled Capacitive-Coupling (DYTONA SOI MOSFET)

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1. Introduction

Floating-body partially-depleted (PD) SOI CMOS technology has come to be utilized for commercial products [1]. Widely accepted advantages over conventional bulk-Si CMOS are reduction of area junction capacitance and elimination of source-to-body reverse bias effect on stacked transistors. In addition, a possibility that transient capacitive-coupling of the body to the gate, source, drain, and substrate improves effective current drivability in CMOS digital logic circuits is discussed [2]. However, one has to take into account negative contribution that parasitic bipolar action due to carrier generation makes off-current at a DC condition increase and that increase of channel impurity concentration to compensate the increased off-current degrades field effect mobility [3].

We analyze floating-body effects of PD SOI MOSFET in terms of effective current drivability in CMOS digital logic circuits. Considering future generation of device scaling, supply voltage is assumed to be low enough to be able to neglect the impact ionization. Based on the analysis, we propose stable enhancement of the effective current drivability by body-tied-to-source operation with high body-contact resistance enough to cause the transient capacitive-coupling. Finally, we verify the stable enhancement by carrying out device simulations.

2. Switching-Steady-State and Body Voltage Overshoot

Dynamics of floating-body charging by body currents is too slow to slave to bias changing during typical switching operation of CMOS digital logic circuits. Therefore, during the switching operation, the floating-body charging little changes and transient capacitive-coupling of the body takes place. After sufficient repetition of the switching operation, the body charging must, however, reach the switching-steady-state where there is no difference in the body charging at the beginning and end of one switching event [2, 4]. The switching-steady-state is defined by the following equation [2, 4]:

$$Q_b(t + t_p) - Q_b(t) = \int [I_{b,total}(V_{gs}, V_{ds}, V_{bs})]dt' = 0, \quad (1)$$

where $Q_b(t)$ is the body charging at an arbitrary time t, t_p is the typical switching period, and $I_{b,total}(V_{gs}, V_{ds}, V_{bs})$ is the total body current at a given set of bias conditions that are the functions of time t'. The integral for t' is taken from the time t to the time $(t + t_p)$.

Equation (1) should be compared with the following equation defining the ordinary-steady-state for DC conditions:

$$I_{b,total}(V_{gs}, V_{ds}, V_{bs}) = 0, \quad (2)$$

where given bias conditions are no longer functions of time. We note that V_{bs} in eq. (1) varies according to the transient capacitive-coupling and differs from V_{bs} in eq. (2). Referring to eq. (2), eq. (1) can be understood as follows: during the switching-steady-state, negative $I_{b,total}(V_{gs}, V_{ds}, V_{bs})$ at the time when V_{bs} transiently overshoots completely compensates positive $I_{b,total}(V_{gs}, V_{ds}, V_{bs})$ at the time when V_{bs} transiently undershoots.

Let us consider NMOS. During pull-down, V_{gs} and V_{ds} increase and the transient capacitive-coupling makes V_{bs} reach its maximum value. At the high V_{bs}, the body-to-source diode is strongly forward-biased. In case of floating-body operation, the large forward diode currents must cause negative $I_{b,total}(V_{gs}, V_{ds}, V_{bs})$. Therefore, V_{bs} can be expected to overshoot during pull-down in CMOS digital logic circuits [2]. By considering in the same manner, V_{bs} in PMOS can be expected to undershoot during pull-up.

3. Drawback of Floating-Body Operation

There are, however, two serious drawbacks of floating-body operation. Consider NMOS. For regular diodes, the extent of forward currents, which constitute negative $I_{b,total}$, is larger than the extent of reverse currents, which constitute positive $I_{b,total}$. Therefore, a small amount of the body voltage overshoot causes the large extent of negative $I_{b,total}$ enough to compensate positive $I_{b,total}$. This means that the body voltage overshoot is not large so much. Moreover, as a ratio of time spent in pull-down to t_p increases, a ratio of time spent in positive $I_{b,total}$, which has to compensate negative $I_{b,total}$ during the body voltage overshoot, to t_p decreases. This means that as input frequency or output load capacitance increases, the body voltage overshoot gradually decreases [2, 5]. We note that these two drawbacks come from the same fact that the extent of currents constituting negative $I_{b,total}$ is larger than the extent of currents constituting positive $I_{b,total}$. Similar drawbacks are seen in PMOS.

The two drawbacks can be suppressed by carrier generation enhancement utilizing the strong impact ionization under relatively high supply voltages [6] or the non-ideal diode with the strong band-to-band tunneling [7]. The casual enhancement of carrier generation, however, accelerates increase of ordinary-steady-state off-current, resulting in increase of channel impurity concentration and in degradation of field effect mobility [3].

4. Body-Terminal-Controlled Capacitive-Coupling (DYTONA)

In order to eliminate the two drawbacks of floating-body operation, we develop a new operation mode of PD SOI MOSFET. The new operation mode utilizes novel transient capacitive-coupling of the body that takes place in body-tied-to-source operation with high body-contact resistance. If body-contact resistance, denoted by R_b, and operating frequency are both enough high, body terminal currents little change body charging during one switching event, resulting in the transient capacitive-coupling. The switching-steady-state for the new operation mode is defined by eq. (1) as well as for floating-body operation.

In addition, if the body terminal currents, denoted by I_b hereafter, are considerably larger than all other components of body currents, $I_{b,total}$ nearly equals to I_b. In this regime, the extent of negative $I_{b,total}$ at $V_{bs} > 0$ nearly equals to the extent of positive $I_{b,total}$ at $V_{bs} < 0$. Because eq. (1) requires that negative $I_{b,total}$ completely compensates positive $I_{b,total}$, V_{bs} during the switching-steady-state can be expected to symmetrically vary around 0 V. This means that the traces of V_{bs} provide high advantages. Moreover, in case of optimized CMOS, $I_{b,total}$ during pull-down is almost completely compensated by $I_{b,total}$ during pull-up. This means that in case of optimized CMOS, body charging during the switching-steady-state is fairly independent of input frequency and of output load capacitance. Therefore, this regime can be expected to eliminate the two drawbacks of floating-body operation.

Another important advantage inheres in this regime. Ordinary-steady-state V_{bs} is nearly 0 V at an arbitrary bias condition, because I_b is considerably larger than all other components of body currents. Therefore, increase of ordinary-steady-state off-current, which results in increase of channel impurity concentration and in degradation of field effect mobility [3], is negligible in this regime.

We call this regime "body-terminal-controlled capacitive-coupling (DYTONA)". The conditions required for DYTONA SOI MOSFET are compiled as follows.

(a) Body-contact resistance is high enough to cause transient capacitive-coupling of the body during switching operation of CMOS digital logic circuits ($R_b >> R_{RC}$).

(b) Almost the entire body charging is controlled by body terminal currents ($I_{b,total} \sim I_b$).

(b') Increase of ordinary-steady-state off-current is negligible (ordinary-steady-state V_{bs} at a standby condition ~ 0 V).

An equivalent circuit model for DYTONA is shown in Fig. 1 as well as for floating-body operation. We note that a concept similar to DYTONA has already been reported [8]. R_b is, however, not high enough to fully satisfy condition (a). Therefore, the transient capacitive-coupling shown in the reports is too weak to considerably enhance effective current drivability.

5. Device Simulation

In order to verify stable enhancement of effective current drivability in DYTONA SOI MOSFET, we carried out two dimensional device simulations. The gate length, equivalent gate oxide thickness, SOI layer thickness, and supply voltage were assumed to be 100 nm, 2 nm, 70 nm, and 1 V, respectively. The impact ionization was neglected. Although we assumed high R_b of 100 MΩ*μm in order to satisfy condition (a), ordinary-steady-state V_{bs} at a standby condition was 0.86 mV and condition (b') was almost satisfied. Our simulations indicated 10 pA/μm order of diode currents including the band-to-band tunneling.

We calculated transient response of NMOS against the trial pulse shown in Fig. 2, which mimicked bias changing in CMOS inverter operated with frequency of 1 GHz. Figure 3 shows transients of body charging during the switching-steady-state, where calculated transients of drive currents have indicated average output load capacitance of 26 fF/μm. Small fluctuations in the body charging indicate strong transient capacitive-coupling of the body caused by high R_b. Decrease in the body charging during pull-down, indicating negative $I_{b,total}$ and V_{bs} overshoot, is almost completely compensated by the increase during pull-up, indicating positive $I_{b,total}$ and V_{bs} undershoot. This trend ensures stable V_{bs} overshoot independent of input frequency and of output load capacitance. Figure 4 shows transients of - I_b (= V_{bs}/ R_b). 1 nA/μm order of I_b considerably larger than the order of the diode currents indicates that condition (b) has been almost satisfied. V_{bs} overshoot during pull-down is expected to be larger than 0.2 V.

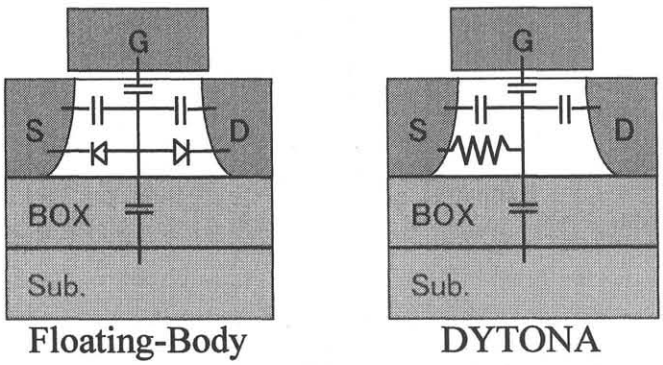


Fig. 1. Equivalent circuit models for floating-body operation and DYTONA. The impact ionization was neglected. According to condition (b), two diodes were eliminated for DYTONA.

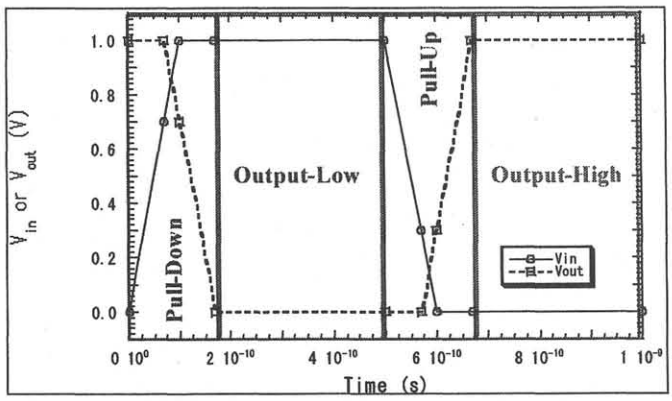


Fig. 2. Trial pulse that mimics bias changing in optimized CMOS inverter. V_{in} and V_{out} indicate V_{gs} and V_{ds} for NMOS, respectively.

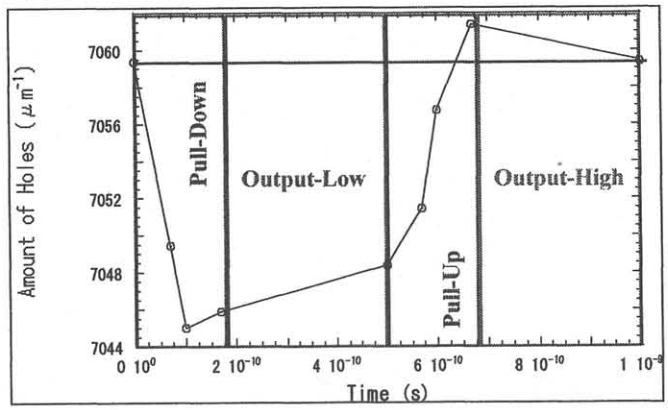
6. Conclusion

We have developed a new operation mode of PD SOI MOSFET called DYTONA and demonstrated that novel transient capacitive-coupling of the body provides stable enhancement of effective current drivability in CMOS digital logic circuits. Further device design for SOI layer thickness must eliminate dependence of body charging during the switching-steady-state on duty cycle or on elapsed time [9], resulting in no history effects.

References

[1] G. G. Shahidi et al.: *ISSCC Tech. Dig.*, 1999, p. 426.
[2] M. Hogyoku: in submitting to Jpn. J. Appl. Phys.
[3] R. Chau et al.: *IEDM Tech. Dig.*, 1997, p. 591.
[4] A. Wel et al.: IEEE Trans. Electron Dev. **45** (1998) 430.
[5] S. Maeda et al.: IEEE Trans. Electron Dev. **45** (1998) 1479.
[6] J. Gautier et al.: *IEDM Tech. Dig.*, 1995, p. 623.
[7] A. Wei and D. A. Antoniadis: *IEDM Tech. Dig.*, 1997, p. 411.
[8] E. Yoshida et al.: *IEDM Tech. Dig.*, 1998, p. 567;
Y. Hirano et al.: *IEDM Tech. Dig.*, 2000, p. 467.
[9] A. Wel et al.: IEEE Electron Dev. Lett. **17** (1996) 391;
H. Mikoshiba and M. Hogyoku: *Ext. Abst. SSDM*, 2000, p. 464.

Fig. 3. Transients of body charging during the switching-steady-state, where there is no difference in the body charging at the beginning and end of one switching event [2, 4].



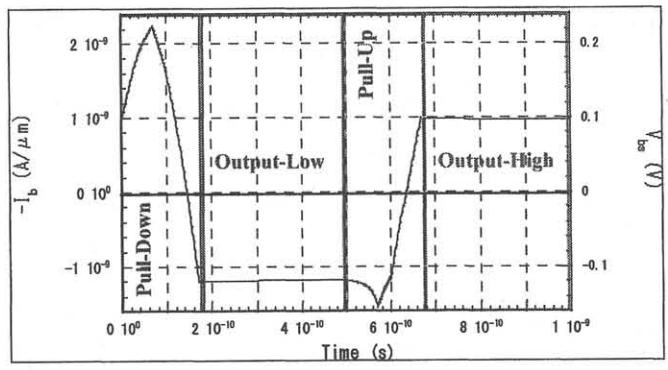


Fig. 4. Transients of - I_b (= V_{bs}/ R_b). During the switching-steady-state, V_{bs} almost symmetrically varies around 0 V.