

## Influences of Gate-Poly Impurity Concentration on Inversion-Layer Mobility in MOSFETs with Ultrathin Gate Oxide Film

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### Introduction

It has been reported that gate oxides thinner than a critical thickness deteriorates the drive current capability [1], strongly suggesting the reduction in inversion-layer mobility. Several scattering mechanisms inherent to ultrathin gate oxides, such as remote Coulomb scattering (RCS) [2,3], have been reported. However, because of the lack of reliable experimental data, the direct evidence of mobility lowering associated with these scattering mechanisms has not been obtained yet. Recently, Takagi and Takayanagi have proposed a modified mobility measurement method, which is applicable to MOSFETs with high gate leakage current [4]. In this paper, we experimentally examine the influences of poly-Si-gate impurity concentration ( $N_{poly}$ ) on inversion-layer mobility ( $\mu_{eff}$ ) in MOSFETs with ultrathin gate oxides ( $T_{ox}$ ) in order to make clear whether or not RCS due to the gate impurities affects  $\mu_{eff}$ . It is found that the mobility is significantly reduced for highly doped gate at  $T_{ox}$  of 1.5 nm or less, strongly suggesting the contribution of RCS due to the gate impurities, which is quantitatively discriminated from that of Coulomb scattering due to substrate impurities and interface states.

### Measurement and Device Fabrication

The split CV method was modified to measure an effective mobility in the MOS inversion layer. The keys are (i) to accurately determine conductance and capacitance even under high gate leakage current and (ii) to evaluate correct surface carrier density ( $N_s$ ) even at a finite drain bias ( $V_d$ ). Since a finite value of  $V_d$  causes the decrease in  $N_s$  near the drain region, the mobility evaluation without any considerations on it has a serious error, particularly in a low field ( $E_{eff}$ ) region [5], in which a mobility lowering occurs as shown later. In this work, Takagi's method [4] was employed in combination with the gate-source and gate-drain capacitance method [5] (Fig.1).

The samples were conventional  $n$ -MOSFETs with an  $n^+$  poly-Si gate. The substrate impurity concentration was left undoped,  $9 \times 10^{14} \text{ cm}^{-3}$ , to minimize the contribution of Coulomb scattering due to substrate impurities. The gate oxides ranging from 1.5 nm to 5.7 nm were pure  $\text{SiO}_2$  film formed by rapid thermal oxidation (RTO). MOSFETs with two  $N_{poly}$  values of  $1 \times 10^{19} \text{ cm}^{-3}$  and  $6 \times 10^{19} \text{ cm}^{-3}$  were prepared by changing arsenic implantation dose. SIMS analysis confirmed that there is no impurity penetration from the poly-Si gate into the Si substrate (Fig.2).

### Results and Discussions

Fig.3 shows the  $\mu_{eff}$ - $E_{eff}$  curve for nMOSFETs with  $N_{poly}$  of  $6 \times 10^{19} \text{ cm}^{-3}$ . The  $\mu_{eff}$  behaviors are identical for  $T_{ox}$  greater than 1.9 nm, though the slight  $\mu_{eff}$  lowering from the universal  $\mu_{eff}$  curve is seen even at  $T_{ox}$  of 5.7 nm. This is attributed to Coulomb scattering due to the charges at the channel/oxide interface. Interface state density ( $D_{it}$ ) of  $7-8 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ , evaluated by the charge pumping method, quantitatively agrees with the  $\mu_{eff}$  lowering ( $\mu_{coulomb}$ ) at  $T_{ox}$  larger than 1.9 nm (Fig.4). The observed higher  $D_{it}$  results from the RTO process.

In MOSFETs with  $T_{ox}$  of 1.5 nm, on the other hand, further  $\mu_{eff}$  lowering is clearly seen, particularly in the low  $E_{eff}$  region. In order to confirm whether this  $\mu_{eff}$  lowering is related to the gate impurities, the mobility for different  $N_{poly}$  of  $1 \times 10^{19} \text{ cm}^{-3}$  was examined. As shown in Fig.5, the  $\mu_{eff}$  lowering is smaller at  $T_{ox}$  of 1.5 nm than that with the higher  $N_{poly}$  (Fig.3). Since other extrinsic factors affecting mobility are the same between the two different values of  $N_{poly}$ , it is concluded that the observed  $\mu_{eff}$  lowering inherent to ultrathin gate oxides becomes more significant with an increase in  $N_{poly}$ .

The mobility-lowering component inherent to ultrathin  $T_{ox}$ ,  $\mu_{lowering}$ , was extracted using the Matthiessen's rule. Fig.6 shows the  $\mu_{lowering}$ - $N_s$  curve as a function of  $N_{poly}$ . It is noted that  $\mu_{lowering}$  at low  $N_s$  is strongly dependent on  $N_{poly}$ . This agrees with the theoretical calculations of RCS (solid lines) including screening effect from free carriers in gate electrode [6], suggesting that the present  $\mu_{lowering}$  associated with ultrathin  $T_{ox}$  is explainable by the framework of RCS. In the higher  $N_s$  region,  $\mu_{lowering}$  is also affected by roughness scattering, resulting in the decrease in  $\mu_{lowering}$  with the increase in  $N_s$  at  $N_{poly}$  of  $1 \times 10^{19} \text{ cm}^{-3}$ . The experimental results at a low temperature strongly suggest that the mobility limited by roughness scattering is degraded at  $T_{ox}$  of 1.5 nm (Fig.7).

### Conclusion

The mobility lowering associated with the gate impurities has been quantitatively evaluated by discriminating the contribution of Coulomb scattering due to substrate impurities and interface states from the total mobility. It was found that the mobility in ultrathin gate oxides lowers significantly for highly doped gate at  $T_{ox}$  of 1.5 nm or less. The present mobility lowering inherent to ultrathin  $T_{ox}$  is explainable by the framework of remote Coulomb scattering, in addition to enhanced roughness scattering.

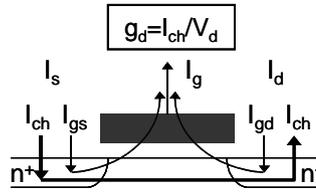
## Acknowledgment

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## I-V characteristics

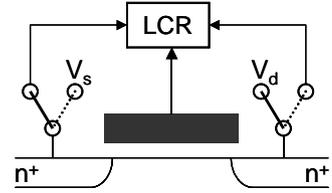


$$I_s = I_{ch} + I_{gs}, \quad I_d = I_{ch} - I_{gd}$$

$$g_d(V_g) = \frac{I_s(V_g) + I_d(V_g)}{2V_d}$$

$$\mu_{eff} = \frac{L}{W} \frac{g_d(V_g)}{qN_s(V_g)}$$

## C-V characteristics



$$C_{gc}(V_g) = C_{gs}(V_g) + C_{gd}(V_g)$$

$$qN_s(V_g) = \int_{-\infty}^{V_g} \{C_{gs}(V) + C_{gd}(V)\} dV$$

Fig.1: Mobility measurement method.  $N_s$  can be determined directly through the CV measurements. It should be noted that the poly-Si-gate depletion effects are correctly incorporated through the CV measurements.

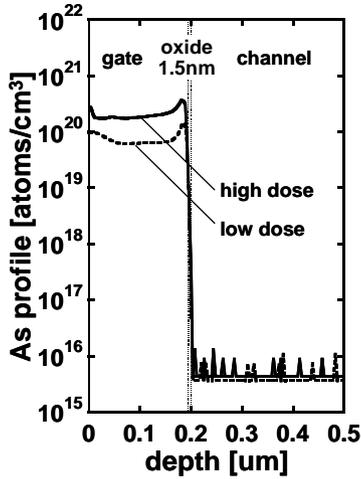


Fig.2: SIMS profile. There is no impurity penetration from the poly-Si gate into the Si substrate.

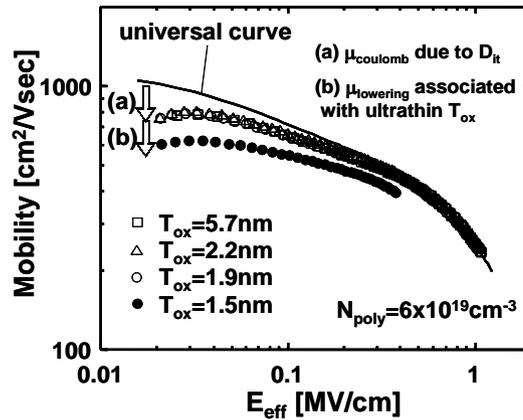


Fig.3: Dependence of  $\mu_{eff}$  on  $E_{eff}$  for MOSFETs with  $N_{poly}$  of  $6 \times 10^{19} \text{ cm}^{-3}$ . Solid line stands for the universal mobility curve.

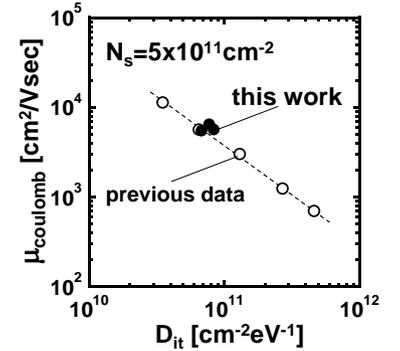


Fig.4: Mobility lowering component limited by Coulomb scattering due to interface states. Open circles stand for the previous data [5] obtained by generating the interface states through FN injection.

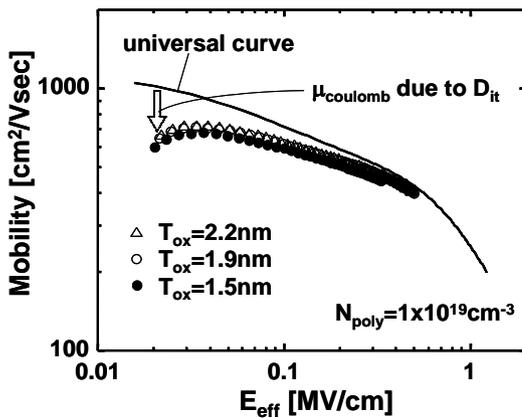


Fig.5: Dependence of  $\mu_{eff}$  on  $E_{eff}$  for MOSFETs with  $N_{poly}$  of  $1 \times 10^{19} \text{ cm}^{-3}$ . Poly gate doping strongly affects  $\mu_{eff}$  at  $T_{ox}$  of 1.5 nm.

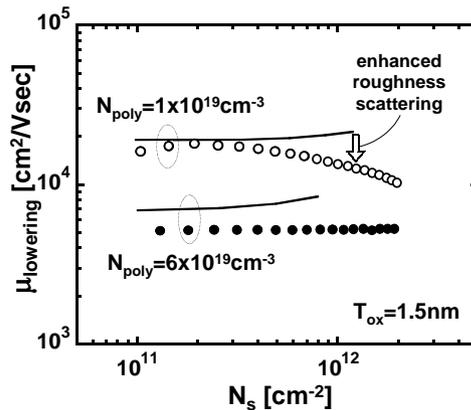


Fig.6: Extracted  $\mu_{lowering}$ - $N_s$  curve as function of  $N_{poly}$ . Solid lines stand for the theoretical calculations [6].  $\mu_{lowering}$  can be explained by the combination of RCS and enhanced roughness scattering.

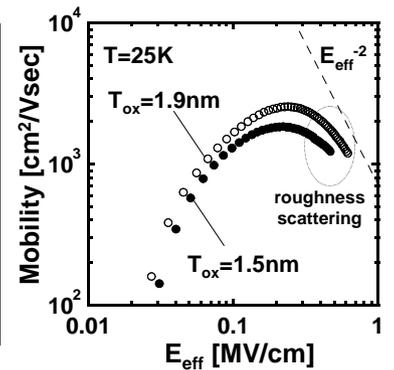


Fig.7: Dependence of  $\mu_{eff}$  on  $E_{eff}$  for MOSFETs at 25 K. The mobility limited by roughness scattering in the high  $E_{eff}$  region is degraded at  $T_{ox}$  of 1.5 nm.