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New Self-aligned Metal-gate MOSFETs Using Aluminum Substitution Technology

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Introduction

For next generation of MOSFETs, low resistivity gate materials are strongly desired. Aluminum is one of a candidate for low resistive materials for MOS gates. On the other hand, aluminum gates cannot endure high temperature annealing at about 900-1100°C used for source drain impurity activation subsequent to the gate fabrication. However, Aluminum Substitution Technology (AST) is expected to overcome this difficulty. This technology enables polysilicon gates that have high temperature immunity to be replaced with aluminum after receiving high-temperature annealing for source drain impurity activation. There are few reports that AST was tried to high performance MOSFETs [1, 2].

In this paper, we present that AST is a more suitable low-temperature technology for the metal gate electrode MOSFETs. The metal/insulator interface characteristics and its reliability are also studied.

Experiment:

Figure 1 shows the process flow for AST to MOSFET gate electrodes. (a) The transistor is fabricated before the forming of multi-layer interconnections. The gate insulation film is made of oxinitride (ON) with a 2.1 nm thick. The gate electrode is made of polysilicon. An opening that leads to the gate electrode is formed on the interlayer insulation film. (b) A 0.4-μm thick aluminum layer for substitution and a 0.2-μm thick Ti layer for substitution acceleration are formed. Various heat treatment steps were done under 450°C for AST. (c) Al and Ti layers are etched to form an interconnection layer. After hydrogen annealing at 400°C, we characterized transistor performances.

Results and Discussion

Figure 2 shows the TEM photograph of a cross-sectional view of Al line by AST. There are no protuberances on Al/SiO_2 interface. The receptivity of the Al substitution gate is 3.45 μΩ cm. The value is almost the same as a pure crystalline aluminum metal. These results show that the substitution aluminum is crystallized (Fig.3). Figure 4 shows the Id-Vg characteristics of NMOSFETs with a 0.1-μm Al and polysilicon gates. The roll-off characteristics of the Al gate are also superior to those of the polysilicon gate (Fig.5). We can show the good characteristics of AST NMOSFET with 2.1 nm gate insulator. Figure 6 shows the results of a simulation regarding f_{max} of an NMOS transistor (with a 90 nm node and a 40 nm gate). It is as low as 1/30 of the sheet resistance of a Co-policided gate ($CoSi_2$ gate). The f_{max} of AST NMOSFET improves about three times of $CoSi_2$ gate MOSFET. Figure 7 shows the C-V characteristics with the AST gate and the polysilicon gate NMOSFETs. The difference of these capacitances stems from the removal of the depletion layer which would be 0.7 nm thick if it were considered as an oxide film. Figure 8 shows the cross section view of 40-nm gate electrode, which is subjected to Al substitution. The SEM images were taken after the Al gate was removed from the gate using sulfuric acid to make the gate hollow. Figure 9 shows the result of FTIR spectrum of SiO_2 (2.2nm- thick)/Si. This spectrum was measured after removing Al substitution on SiO_2/Si. The spectrum was the same with the oxidized SiO_2 layer. This shows that thin SiO_2 layer under Al-gate is not damaged by AST. Figure 10 shows the comparison of subthreshold factors (s-value). This shows the interface between Al substitution gate and insulating layer does not produce the defect states. Figure 11 shows the annealing time dependence on Id and Ig of a 350°C AST NMOSFET (Lg=0.1um). Vg and Vd are 1V, respectivly. The annealing temperature was 400°C. Id and Ig show no degradation after thermal annealing. Figure 12 shows an estimation of the lifetime of AST NMOSFETs with a 2.1-nm ON gate insulation film. The lifetime for 10 years of the ON gate insulation film in the Al substitution gate is guaranteed under an electric field intensity of 8 MV/cm.

Conclusion

The use of AST has proved to achieve new metal-gate MOSFETs at a low temperature process. AST NMOSFETs ensure superior electrical characteristics, high heat resistance and sufficiently lifetime. It will be useful for f_{max} improvement. It seems that AST will play an important role in a low temperature metal gate fabrication in the age of miniature gates of 0.1 μm and under.

Acknowledgement

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References:

[1] H. Horie, M. Imai, A. Itoh, Y. Arimoto, IEDM Tech. Dig., 946(1996).
[2] S. Nakamura, R. Suzuki, M. Fukuda, M. Kobayashi, A. Hatada, Symp. on VLSI Tech., p.35, 1999.

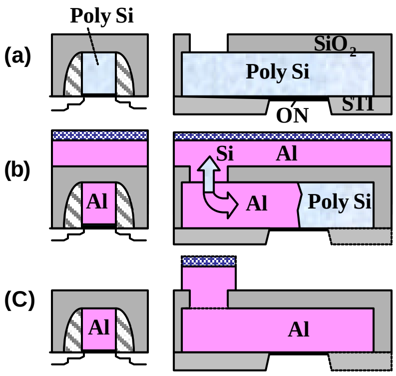

Figure 1. A schematic illustration of process flows. (a) Opening of gate contact hole after the transistor fabrication (b) Annealing for AST after deposition of Al and Ti layers (c) Etching of Al and Ti layers for fabrication of interconnections.

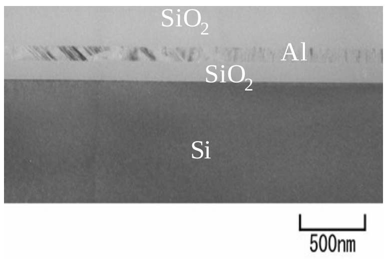

Figure 2. Cross-section TEM image of Al layer on SiO$_2$ layer after AST process.

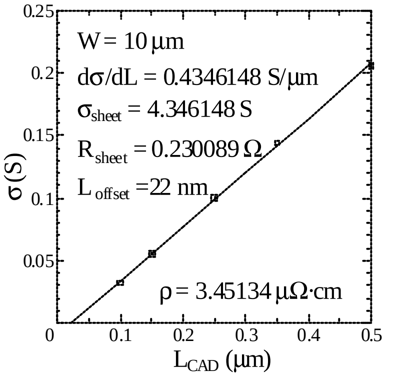

Figure 3. Conductivity and resistively of the Al-gate. The resistivity of the Al-Gate is 1/30 of that of a $CoSi_2$-gate.

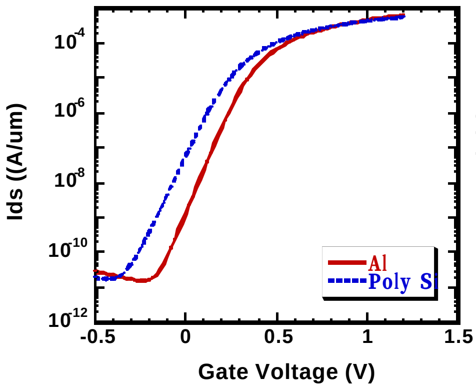

Figure 4. Id-Vg characteristic of 0.1 μm Al-gate NMOSFETs.

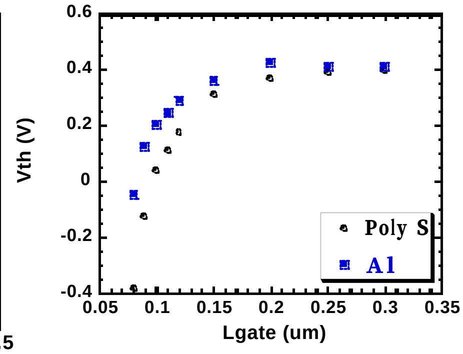

Figure 5. Comparison NMOSFETs V_{th} roll-off characteristics with Al-gate and N poly Si gate. Al-gate roll-off characteristics is superior to N poly Si gate one. AST anneal is done at 350℃.

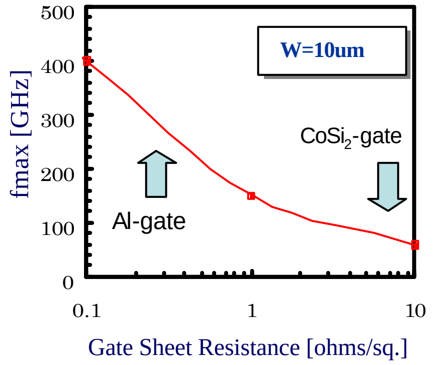

Figure 6. Simulation results for f_{MAX} of Al-Gate NMOSFET. It is possible to increase the f_{max} of Al-Gate NMOSFET about three times.

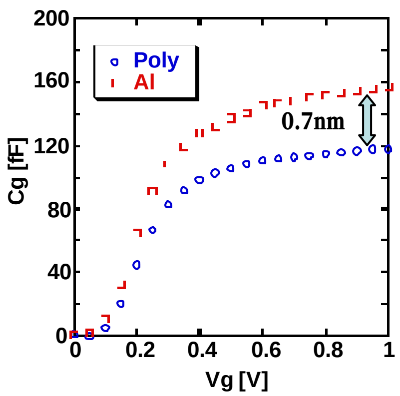

Figure 7. Comparison of NMOSFET C-V characteristics with Al-gate and N poly Si gate. The use of Al gate eliminates a depletion layer that is 0.7 nm if considered as an oxide film.

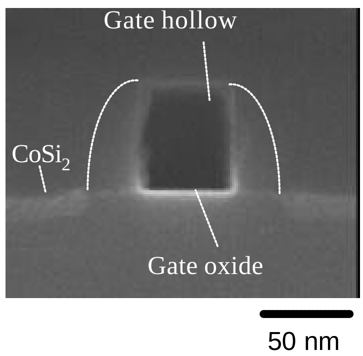

Figure 8. Cross-section SEM image of Al gate after Al removing using wet etching. Gate length is 40nm.

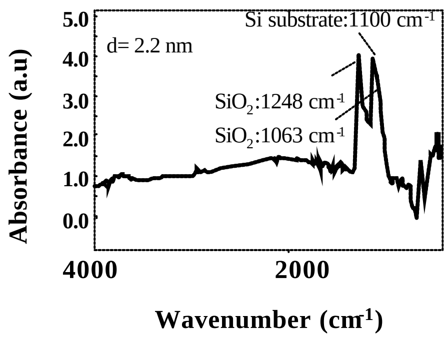

Figure 9. IR spectrum of SiO_2/Si after Al removing.

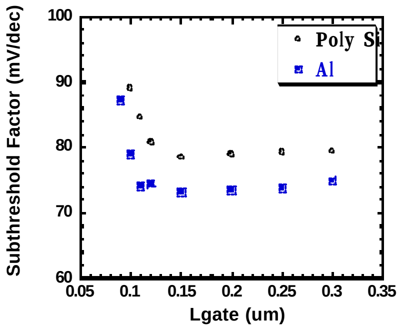

Figure 10. Comparison of NMOSFETs subthreshold factor with Al-gate and N poly Si gate. AST annealing is done at 350℃.

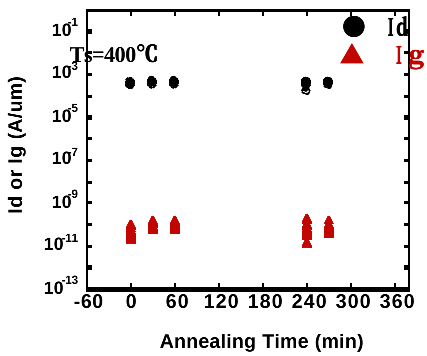

Figure 11. Comparison of Id and Ig @1V of Al gate NMOSFETs. Annealing is done in N_2 atmospheric pressure.

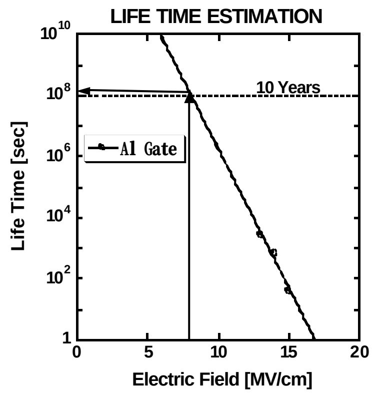

Figure 12. Lifetime estimation for AST NMOS. 2.1nm-ON film under the Al gate can keep 10 year-life at 8MV/cm.