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High Performance Poly-Si Device with Thin Gate Oxide Film Grown by Plasma Oxidation Technology

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1. Introduction

In future poly-Si devices, it is necessary to realize high quality gate oxide process at low temperature. A conventional oxidation process causes the silicon interface micro-roughness and large interface trap density. In this work, polyoxide films are grown by oxygen radical (O*) which is generated by microwave excited high-density plasma technology at 400°C[1,2]. We succeeded to fabricate high quality poly-Si device with lower leakage current and larger drain current by using this plasma process.

2. Experimental

Poly-Si devices were fabricated. 800nm thickness of amorphous Si (a-Si) was deposited by LPCVD. This a-Si was crystallized by annealing (650°C, 6hours) in N_2 ambient. After annealing, we got large grain by using the wet oxidation (1000°C). The grain size was 500nm. We removed SiO_2 after the wet oxidation by diluted HF etching. The gate oxide film (11.8nm) of conventional device was formed by the dry oxidation at 1000°C. The other gate polyoxide film (7.46nm) was grown by Kr/O_2(97/3) microwave (2.45GHz) excited high-density ($>10^{12}$ cm^{-3}) plasma technology at 400°C. P-doped poly-Si gate electrode was deposited by LPCVD and annealed at 800°C for 30min. Source/Drain of MOSFET was formed by the ion implantation (As^+, BF_2^+:25keV-1.5 x 10^{15} cm^{-2}) and the post implantation annealing at 800°C for 30min.

3. Results and Discussion

Fig.1 shows the atomic force microscope (AFM) images (5μm×5μm) of the (a) bare poly-Si film surface (before polyoxide film growth), (b) poly-Si surface after removed SiO_2 formed by the O* oxidation (400ºC), (c) poly-Si surface after removed SiO_2 of the dry thermal oxidation (900ºC). Both (b) and (c) are grown on poly-Si films. The textures of Fig.1 (a) and (b) exhibit similar structure because the low polyoxide growth temperature (400°C) causes only small changes in the grain size of the underlying poly-Si film. Fig.1(a) and (c) show significant change in the surface texture, which is caused by two factors. The first is the migration of Si atoms and the regrowth of the grain on the poly-Si film due to the high polyoxide growth temperature (1000ºC). The second is that the dry oxidation has crystal orientation dependence.

Fig. 2 shows the stress in poly-Si surface region. The initial stress in the poly-Si surface region is 3 x 10^{19} [dyn/cm^2] as tensile. The stress in poly-Si changes tensile to compression by the dry oxidation (1000°C). The changing of stress direction in poly-Si causes the roughed surface as shown in Fig.1 (c). However, the O* oxidation does not cause a large stress because of the low temperature. So, the poly-Si surface can keep flat and the regrowth of grain and migration of Si atoms do not occur.

Fig.3 (a) and (b) show the Id-Vg characteristic for NMOS(a) and PMOS(b). The drain current of device with the O* oxide (7.46nm) is larger than that with the dry oxide (11.8nm).

Fig. 4(a) and (b) show the transconductance (Gm) for NMOS and PMOS, respectively. In fig. 4(a) and (b), the transconductance with the device formed by the O* oxidation is 3 times larger than that by the conventional dry oxidation.

Fig.5(a) and (b) show Id-Vg characteristics for device with the dry oxide and the O* oxide, respectively. These characteristics were measured at various temperatures. The drain current of the device with dry oxide increases with an increase of all measured temperatures. However, the drain currents (77K and 150K) of device with O* oxides are the same. That is the reason why many electrons are captured by trap sites in the channel region generated by dry oxidation. The drain current of the devices with the O* oxide is larger than that with the dry oxide at low temperature region (77K and 150K).

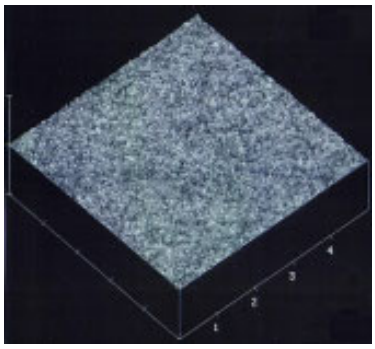
Fig.6 shows schematic energy-band diagram of poly-Si device in channel region. The exist of electron traps forms energy barrier against conductive electrons. The energy barrier increases with the number of electron traps. The high energy barrier disturbs the drain current in channel region. It is suggest that the drain current of the device with the O* oxide is larger than that with the dry oxide.

4. Conclusion

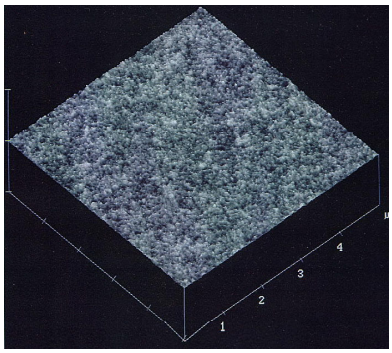
Polyoxide film with the O* oxide at 400°C was demonstrated high quality poly-Si device electrical properties in terms of reduced leakage currents and higher drain currents. We explained the dependence of temperature about the drain current changed by poly-Si surface. We succeeded to decrease surface roughness and electron trap and fabricate very useful high performance poly-Si device with thin gate oxide film grown by plasma oxidation technology.

References

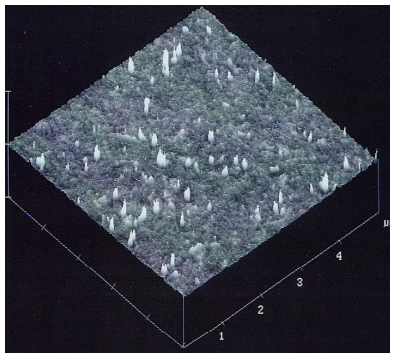
[1] M. Hirayama, et al., IEDM Tech. Dig., p249(1999)
[2] K. Sekine, et al., Symp. VLSI Tech., p115(1999)



(a)Bare poly-Si surface (before oxidation)
Rmax :10.772nm Ra:0.959nm



(b)O* oxidation (400°C)
Rmax :9.189nm Ra:0.738nm



(c) DRY oxidation (900°C)
Rmax :42.733nm Ra:1.277nm

Fig.1 AFM images of the polyoxide/poly-Si interface after removed SiO_2.
After dry oxidation, the poly-Si surface is roughed. The surface is not changed by O* oxidation.

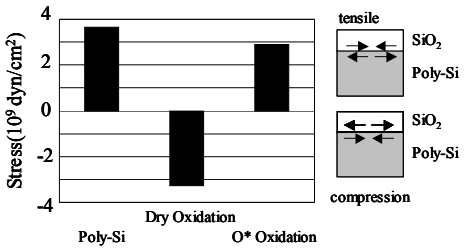
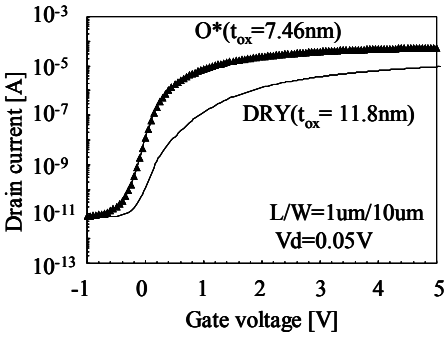
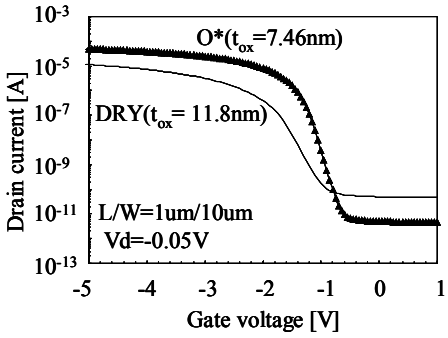


Fig.2 Stress in the poly-Si surface region before and after gate oxidation. The stress after dry oxidation changed drastically compared to initial surface.

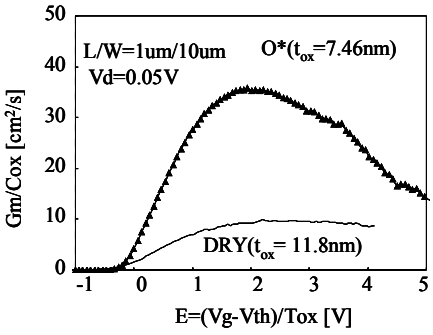


(a) NMOS

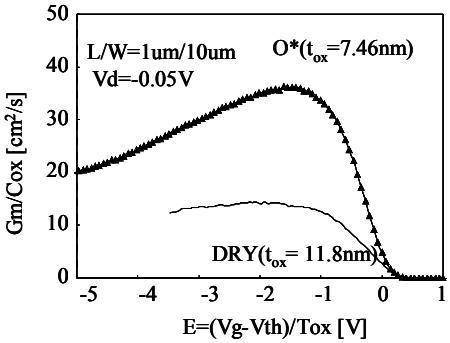


(b) PMOS

Fig.3 Id-Vg characteristics for NMOS(a) and PMOS(b). The Drain Current of both device with O* oxidation are larger than that with the dry oxidation.

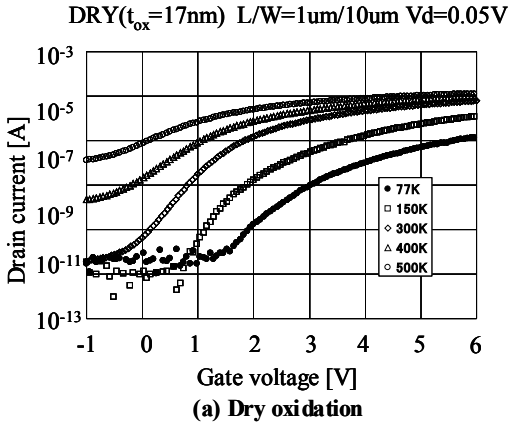


(a) NMOS

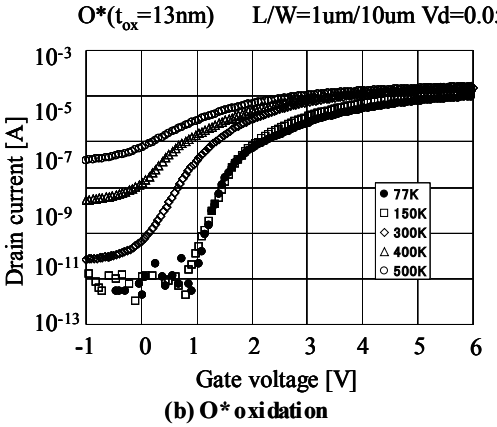


(a) PMOS

Fig.4 The transconductance (Gm) of MOSFET as a function of the electric field across the gate oxide. The Gm value of both NMOS and PMOS with the O*oxide are much lager than those with dry oxide.



(a) Dry oxidation



(b) O* oxidation

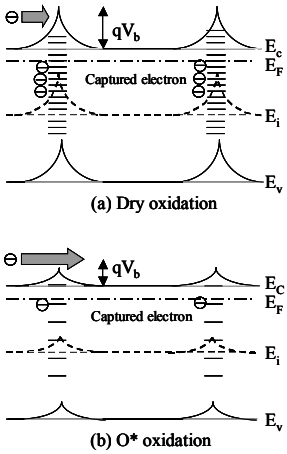


Fig.5 Id-Vg characteristics. This characteristics were measured at various temperature. The grain size is 100nm. The drain current of the device increases with an increase of all measured temperature.

Fig.6 Schematic energy-band diagram of poly-Si device. The exits of electron traps forms energy barrier against conductive electrons in channel region.