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# A Novel High Performance Power MOSFET with Split well and Split Poly Structure

Feng-Tso Chien[1], Kou-Way Tu[2,3], Shin-Tzung Su[2], Ching-Ling Cheng[2], Dung Jen-Huie[2], Chung-Yuan Kung[3],and Yen-Chih Huang[3]

[1]Dept. of Electronic Engineering, Feng Chia University, Taichung, Taiwan 32054, R.O.C

Phone: +886-4-24517250 ext 4579 E-mail: ftchien@fcu.edu.tw

[2]R&D Dept., Chino-Excel Technology Corp.,Chung-Ho,Taiwan ,R.O.C.

[3]Dept. of Electrical Engineering, Chung Hsing University, Taichung, Taiwan, R.O.C

## 1. Introduction

A low gate charge Power MOSFET with spilt P-well and split poly has been fabricated. Drain breakdown voltage and on-state resistance are two of the most important issues in Power MOSFETs design. In order to achieve a high drain-source breakdown voltage($V_{br}$), some junction termination technologies such as mesa etch and beveling, floating guard rings, field plates, and V-groove guard rings are general methods to apply in junction termination [1, 2].

In addition, a high frequency capability Power MOSFET, which requires low resistance($R_{on}$) and low gate charge($Q_g$), plays an important rule in high speed applications. However, high $V_{br}$, low $R_{on}$, and high speed operation are trade-off issues in power MOSFETs design. In order to further improve the performance of power MOSFETs, we proposed a split poly and split p-well structure, which can reduce the $R_{on}$ and $Q_g$ without scarifying $V_{br}$.

A split poly design, which minimizes the overlap area between the gate the drain, can reduce the input capacitance as well as the $Q_g$ of a power MOSFET. In addition, an n+ implant is applied in the split poly region to reduce the parasitic JFET effect resistance. Split p-well with a heavy p+ region design can relocate the breakdown point and decrease the parasitic bipolar effect. In addition, the unclamped inductive switching performance can also been further improver in this design.

## 2. Device design

Device and process simulator “MEDICI” and “TSUPREM-4” are used to design a power MOSFET with a $V_{br}$ of 500V by field plates and floating guard ring technologies.

Fig.1 shows the cross-section of split poly and split p-well structure. Fig. 2 (a) shows the top view diagram of conventional and split poly design, and fig. 2 (b) shows the photograph of split poly device. In this study, split poly and split well structure is compared with the conventional design. Although split poly and n+ implant in split poly region might shift breakdown point toward to the surface, the split p-well design can avoid that happen and relocate breakdown point on the middle of p-well[3]. In addition, we reduce the poly width to ensure a high

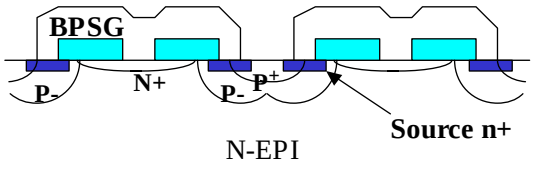
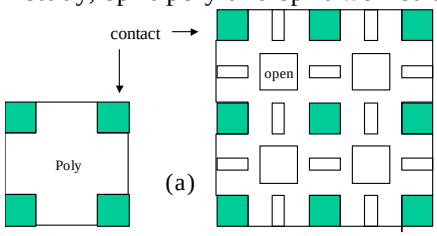



Fig. 1 cross-section of split poly and split p-well structure



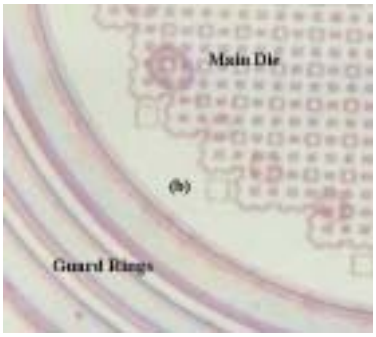




Fig. 2 Top view diagram (a) and photograph (b) of split poly structure

$V_{br}$. All the devices in our design have the same die size of $3500^2$ $\mu m^2$.

## 3. Device Fabrication and Performances

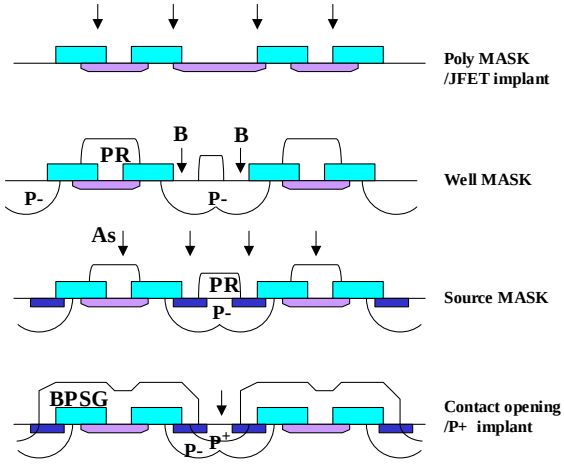



Fig. 3 Process flow of split poly and split p-well device

Fig. 3 illustrates the process flow to fabricate the device. Simulated and measured data shows the Vth of both devices are all the same. Fig. 4 shows the devices on-state characteristics. The $R_{on}$ is 514mΩ and 693mΩ–$cm^2$ for split structure device and convention one, respectively. It can be seen the split structure device have a lower $R_{on}$. Fig. 5 shows the simulated on state current density of these two devices. It is obviously that the split structure device has a large current density in the split poly region, and therefore, the $R_{JFET}$ can be reduced.

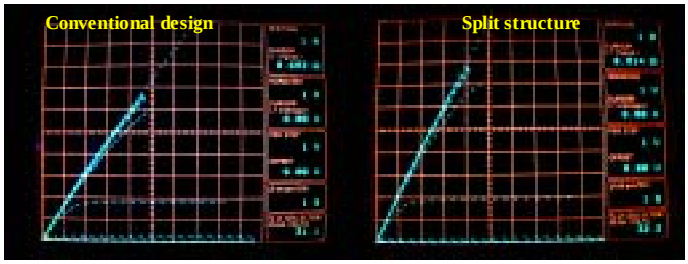



Fig. 4 On state characteristics of conventional and split structure devices

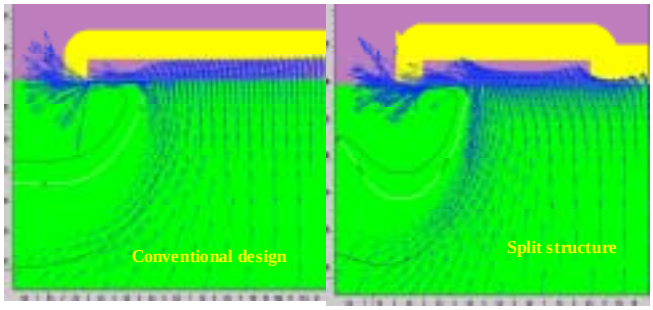



Fig. 5 Simulated current density comparison between conventional and split structure devices

Since split poly structure can reduce the overlap area between the gate the drain, therefore, the input capacitance of a power MOSFET can be reduced. Fig. 6 shows simulated and measured $Q_g$ performances W/ and W/O split poly structure. The time axis (measured) can be easily replaced by the gate charge. The $Q_g$ are measured under a Vgs = 10V, Vds = 400V and Ids = 10A. The $Q_g$ performance can be further improved by split poly design, especially at gate-drain charge ($Q_{gd}$), which is the most important item for switching characteristics. The averaged gate source charge ($Q_{gs}$), $Q_{gd}$, $Q_g$, for W/ & W/O split structure are 5.8 nC, 12 nC, 30 nC and 7.8 nC, 28 nC, 54 nC, respectively. The reduced gate charge characteristics can ensure device to operate at a high

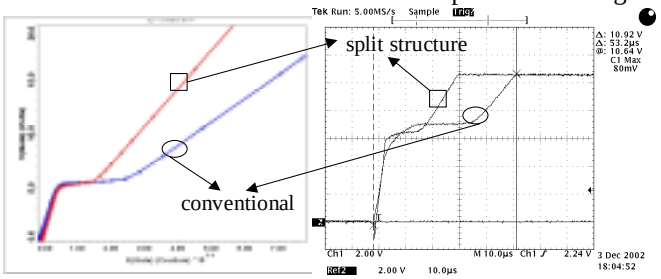



Fig. 6 Gate charge performance W/WO split poly

frequency and switching operation.

## 4. Conclusions

A 500V Power MOSFET structure with split p-well and split poly has been proposed and discussed. Split p-well with a heavy p+ region design can relocate the breakdown point as well as release hot spot effect, and therefore improve device reliability. Split ploy with proper implant technology can reduce JFET effect, and improve the $R_{on}$ performance of Power MOSFET. In addition, the $Q_g$ performance can be reduced to half as comparing with the original design. Combining split p-well and split poly design of Power MOSFT, the performance of this device can be further improved.

## References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