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Enhancement of V_{TH} Degradation under NBT Stress due to Hole Capturing

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1. Introduction

Negative bias temperature instability (NBTI) has become increasingly serious in the context of efforts to realize highly reliable integrated CMOS devices, because of the severe degradation of threshold voltage shift and interface-state generation [1]. The threshold voltage shift is generally attributed to the creation of interface traps and positive fixed charges consequent on the dissociation of Si-H bonds at Si/SiO_2 interface by holes, and subsequent diffusion of the released hydrogen-related species towards the gate electrode [2-5]. However, the mechanism of NBT degradation has not yet to be fully clarified.

In the work reported in this paper, the origin of V_{TH} degradation was investigated by applying alternate negative and positive BT stress. As a result, the enhancement of V_{TH} degradation due to hole capturing in gate oxide film has been observed.

2. Experiment

The devices used in this study were P-channel MOSFETs having SiO_2 and SiON films as gate oxides. Oxide thickness of SiO_2 films used in this work is 2.3 and 5.7 nm. The dimension of MOSFET is 20μm of gate width and 1 μm of gate length. Fig. 1 shows the schematic diagram of the experimental condition in this work. NBT (in the inversion condition) and PBT (in the accumulation condition) stress were alternately applied. V_G-I_D measurement and charge-pumping current measurement were performed during respective stress.

3. Results and Discussion

Fig. 2 shows V_{TH} and Dit in the case of thick (5.7 nm) SiO_2 films under alternate NBT and PBT stress. Note that V_{TH} shift after NBT stress is recovered by applying PBT stress. In addition, the recovery after 2nd PBT stress is smaller than that after 1st PBT stress. On the other hand, Dit increases by NBT stress, but there is no change in Dit during PBT stress. This result suggests that V_{TH} shift under NBT stress contains the reversible process, and that interface-state generation under NBT stress is irreversible process.

The recovery of V_{TH} depends on the applying positive bias. Fig. 3 shows the recovery ratio of V_{TH} in the case of thick SiO_2 films as a function of PBT stress time. The recovery ratio is estimated as the ratio of V_{TH} under NBT stress (V_{TH_NBT}) for 5120 sec at V_G=-4.2V to that under PBT stress (ΔV_{TH}^{+}). From this experimental result, it is suggested that the strength of positive bias plays an important role for the reversible process of V_{TH}.

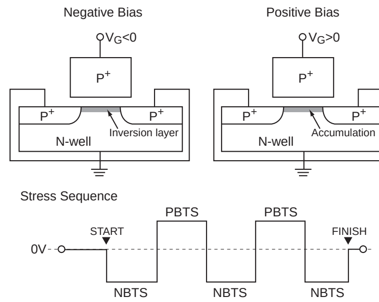

Fig. 1 Schematic diagram of experimental condition. In this work, NBT (in the inversion condition) and PBT (in the accumulation condition) stress were alternately applied.

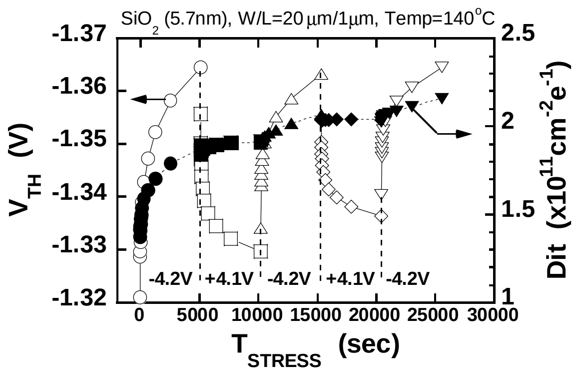

Fig. 2 Threshold voltage shift (V_{TH}) and generated interface-state density (Dit) under alternate NBT and PBT stress. Oxide thickness is 2.3 nm. Note that the recovery of ΔV_{TH} is observed under PBT stress, though there is no change in Dit during PBT stress.

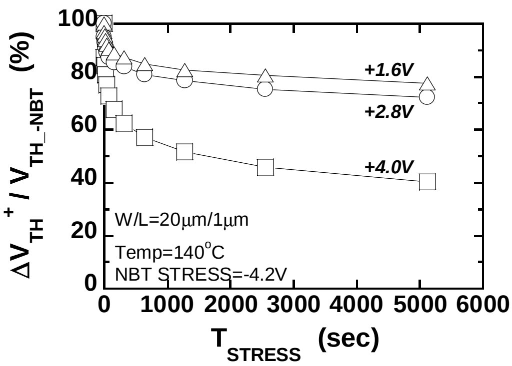

Fig. 3 Recovery ratio of V_{TH} by applying PBT stress. The recovery ratio is estimated as the ratio of V_{TH} under NBT stress to that under PBT stress. NBT stress was performed under V_G=-4.2 V for 5120 sec. It is found that the recovery ratio strongly depends on V_G of PBT stress.

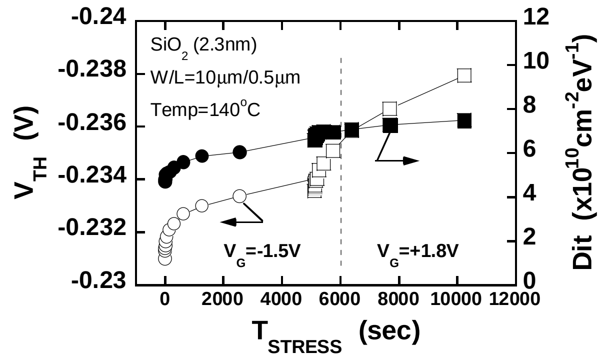

Fig. 4 Threshold voltage shift (V_{TH}) and generated interface-state density (Dit) under alternate NBT and PBT stress. Oxide thickness is 2.3 nm. Note that V_{TH} and Dit monotonically increase even under PBT stress.

Fig. 4 shows V_{TH} and Dit in the case of thin (2.3 nm) SiO_2 films under alternate NBT and PBT stress. Under PBT stress, V_{TH} shift significantly increases instead of the V_{TH} recovery. Furthermore, it is found that Dit monotonically increases in spite of NBT and PBT stress.

On the basis of the experimental results, the reversible and irreversible process of NBT degradation is discussed. From the result that the recovery of V_{TH} strongly depends on V_G of PBT stress, charged species relate to the reversible process in V_{TH} shift. On the other hand, ionic hydrogen-related species, *i.e.* H^+, H_3O^+ and so on, probably have no relation to the recovery of V_{TH}, because no change in Dit during PBT stress was observed. Therefore, it is inferred that the capture and release of holes due to applying V_G cause to the reversible process in V_{TH} shift. In the case of thick SiO_2 films, it is confirmed that the gate leakage current is less than 100 pA. This means that holes and electrons cannot tunnel through SiO_2 films. Therefore, holes from the inversion layer are captured in the gate oxide, while the interface-states are generated by inversion holes as schematically shown in Fig. 5 (a). These captured holes are released, when the reverse positive bias is applied. Thus, it is inferred that the recovery of V_{TH} is observed. On the other hand, in the case of thin SiO_2 films, holes directly tunnel through SiO_2 films. Electrons also tunnel from N-well under applying positive gate voltage as shown in Fig. 5 (b). It is inferred that these electrons generate defects in SiO_2 films, and holes from the valence band of the gate electrode are captured at these defects. Therefore, V_{TH} also shifts under PBT stress.

Finally, the case of thin SiON films is shown in Fig. 6. It should be noted that the recovery of V_{TH} shift is clearly observed in spite of the same thickness with the case of thin SiO_2 films shown in Fig. 4. This experimental result suggests that ,in the case of SiON films, the nitrogen-related hole capturing enhances V_{TH} shift under NBT stress, which may become a fatal issue for CMOS technologies.

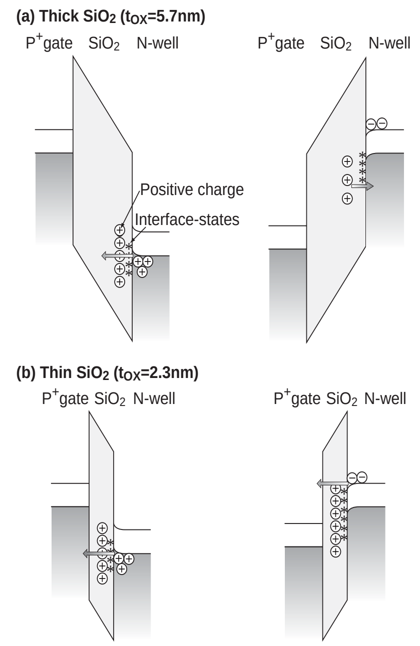

Fig. 5 Schematic diagram of V_{TH} and Dit degradations under alternate NBT and PBT stress comparing thin and thick SiO_2 films. In the case of thick SiO_2, holes captured in SiO_2 under NBT stress are released by applying positive bias. Therefore, the recovery of V_{TH} shift is observed.

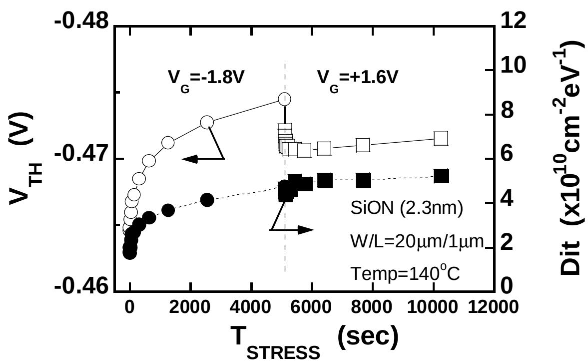

Fig. 6 Threshold voltage shift (V_{TH}) and generated interface-state density (Dit) of thin SiON films under NBT and PBT stress. It is found that the recovery of V_{TH} shift is clearly observed even though oxide thickness is 2.3 nm.

4. Conclusion

In this work, the changes of V_{TH} and Dit under alternate NBT and PBT stress have been investigated. As a result, the reversible V_{TH} shift is observed not only in the case of thick SiO_2 but also thin SiON. It was also found that the recovery of V_{TH} strongly depends on the applying reverse positive bias, and that no significant change of Dit under PBT stress is observed. On the other hand, in the case of thin SiO_2 films, V_{TH} and Dit monotonically increase even under PBT stress. From these results, it was suggested that nitrogen-related hole capturing enhances V_{TH} degradation in the case of SiON films.

References

[1] N. Kimizuka *et al.* :VLSI Symp. Digest, 73, 1999.
[2] N. Kimizuka *et al.* :VLSI Symp. Digest, 92, 2000.
[3] G. La. Rosa *et al.*: IRPS proc., 73, 1999.
[4] T. Yamamoto *et al.* : IEEE ED-46, 921, 1999.
[5] G. J. Gerardi *et al.* : J. Electrochem., 2609, 1989.