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New Mechanism for Negative-Bias-Temperature Instability and Its Impact on Scaling of pMOSFETs

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Abstract

Negative-bias-temperature instability (NBTI) of pMOSFETs with ultra-thin gate dielectric is characterized. A new mechanism due to trapping of holes in the nitride/oxide (N/O) stack during bias-temperature stressing (BTS) was identified. Threshold voltage (Vth) shift caused by BTS was found to recover after BTS stressing. Such mechanism becomes more significant as channel length is scaled down, and could be important for future high-k gate dielectric applications.

Keywords: NBTI, N/O stack, hole trapping, Vth recovery, pMOSFET.

Introduction

N/O stack is a potential candidate for replacing oxide as the gate dielectric of CMOS devices in the near future. Comparing to thermal oxide, N/O stack can effectively reduce leakage current and suppress B penetration without compromising the dielectric/channel interface quality [1]. For practical applications, however, the reliability issues need to be thoroughly addressed. In this work, we investigate the negative-bias-temperature instability (NBTI) of p-MOSFETs, a potential bottleneck of device lifetime [2]~[3]. It is generally believed that the generation of positive fixed charges and interface states are responsible for the Vth shift and drain current degradation after BTS [2]~[5]. It was also found that nitrogen incorporation at or near the oxide/channel interface could further aggravate NBTI [2]~[5]. In this work, we show a new important mechanism affecting the NBTI performance of devices with N/O stack.

Experimental

Test devices were fabricated using 0.13 μm CMOS technology (see Table 1). Three types of gate dielectric, i.e., thermal oxide, nitrided oxide, and N/O stack, were compared in this work. The nitrided oxide received a high-temperature anneal in NO gas after the base oxide formation. In contrast, the N/O stack was obtained by depositing a CVD nitride layer on the base oxide. The equivalent oxide thickness (EOT) is about 1.6 nm, as extracted by a CV simulator that takes into account quantum mechanical and poly gate depletion effects.

The bias-temperature (BT) stress was performed at 150 ^{o}C under a gate bias of –2 V, with all other electrodes (S/D and well) grounded. The characterization procedure is shown in Fig. 1.

Results and Discussion

Jg-Vg characteristics for all splits are shown in Fig. 2. It can be seen that the use of N/O stack effectively reduces the gate leakage, implying the strength of oxide field in the N/O stack is lowered. Fig. 3 shows the Vth shift as a function of stress time. It is observed that the N/O splits exhibits beetter NBTI resistance than the nitrided oxide split. This is mainly ascribed to the reduced oxide field mentioned above. Fig. 4 shows the Vth shift (i.e., Vth difference between the testing time points 2 to 3 in Fig. 1) as a function of channel length (L). The magnitude of Vth shift increases with decreasing channel length, consistent with previous reports [2][4]. Still, N/O stack devices exhibit higher immunity than the nitrided oxide devices.

We also observed that, for devices with N/O stack gate dielectric, Vth could recover after 2 days of storage at room temperature as shown in Fig. 5. Such phenomenon is not significant, however, for the nitrided oxide (Fig. 6), and is negligible for pure oxide (Fig. 7). This indicates the existence of a new NBTI mechanism for N/O stack. It could be related to the trapping of holes in the nitride or nitride-oxide interface [6]. Holes trapped during BTS could relax through the ultra-thin base oxide after BTS, resulting in the recovery phenomenon. Note that Id-Vg characteristics were measured at room temperature (time points 4 and 5, Fig. 1), though similar behavior was also observed when Id-Vg characteristics were measured at time points 3 and 6.

Fig. 8 shows the amount of Vth recovery (i.e., Vth difference between time points 4 & 5) as a function of channel length. The recovery phenomenon is found to be more pronounced with shorter channel length. This could be explained as follows: (1) The results shown in Fig. 4 imply that the density of trapped holes in N/O stack increases with decreasing L, it is therefore reasonable to expect that the de-trapping of holes after BTS also increases with decreasing L. (2) Band-diagrams shown in Fig. 9 indicate that, due to opposite electric field in the oxide, trapped holes over the channel regions have a lower possibility to return to the substrate than those over the S/D extension regions.

To further understand the impact of such NBTI mechanism on the device operation, we performed a 2nd BTS (Fig. 1) on several samples. Fig. 10 shows the data of ΔVth for a device with N/O stack as a function of total stress time. The “dip” in data at the beginning of the 2nd BTS is due to relaxation of holes during the break period. After a short time, however, the ΔVth jumps to join the line extrapolated from the data in the 1st BTS period, indicating the re-trapping of holes.

Conclusion

By optimizing the nitride and/or N/O interface quality, further improvement in the NBTI immunity is possible. However, a new NBTI mechanism due to trapping of holes in N/O gate dielectric is identified. The newly-discovered mechanism could also be crucial for future high-k gate dielectric applications, since most high-k dielectrics contain a number of trapping centers and are usually stacked on an interfacial oxide [7], structurally resembling the N/O stack explored in this work.

Acknowledgments

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Table 1: Process sequence of the test devices.

*	Shallow trench isolation
*	Well/channel implantation
*	**Gate dielectric preparation**
	Split 1: thermal oxide
	Split 2: base oxide + High-T NO-gas annealed (nitrided oxide)
	Split 3: base oxide + CVD nitride (N/O stack)
*	Poly-Si deposition and doping
*	Gate patterning
*	S/D extension / Halo implant
*	Gate sidewall formation
*	S/D implant and RTA

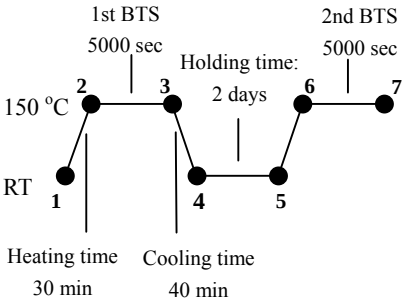

Fig. 1 Experimental procedure for characterizing the test devices.

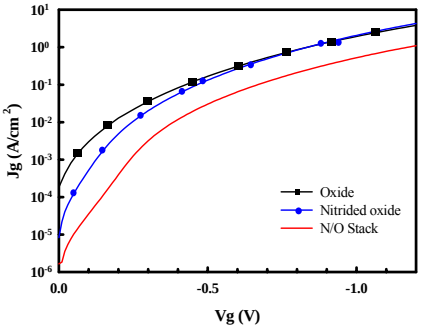

Fig. 2 The Jg-Vg characteristics for all device splits.

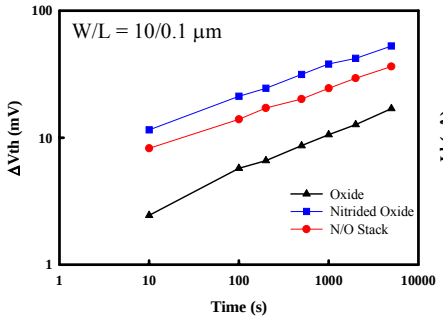

Fig. 3 Time dependence of Vth shift during 1st BTS.

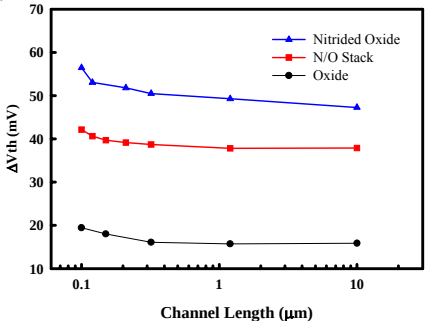

Fig.4 Vth shift between time points 2 and 3 as a function of channel length.

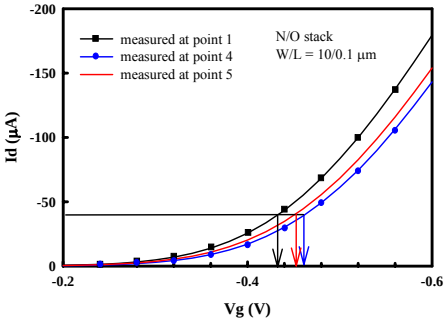

Fig. 5 Ig-Vg characteristics for N/O stack spit measured at time points 1, 4, and 5.

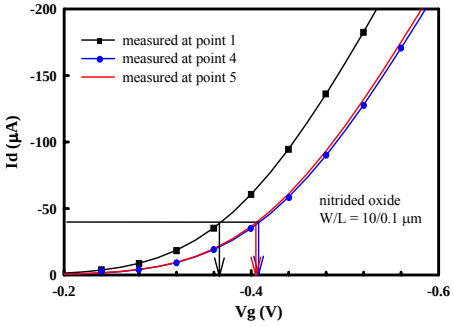

Fig. 6 Ig-Vg characteristics for nitrided oxide split measured at time points 1, 4, and 5.

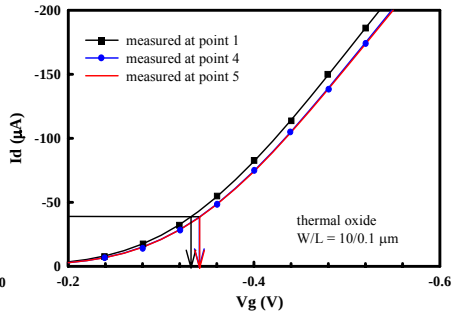

Fig. 7 Ig-Vg characteristics for oxide split measured at time points 1, 4, and 5.

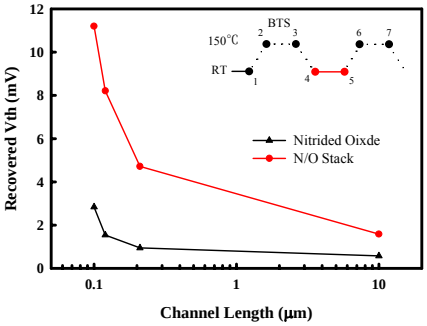

Fig.8 Vth recovery as a function of channel length.

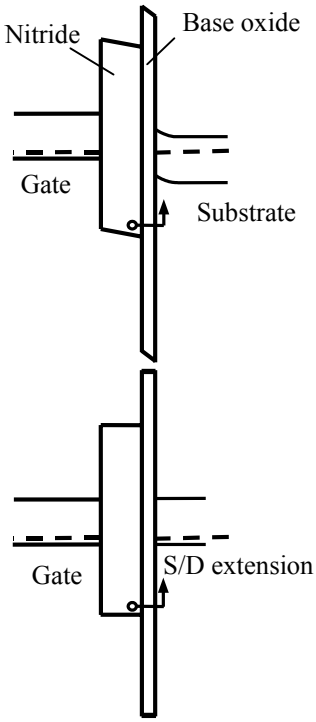

Fig. 9 Band diagrams at (top) channel and (bottom) S/D extension regions (Vg = 0).

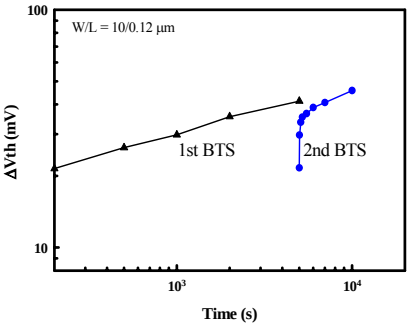

Fig. 10 Vth shift as a function of total stress time for a device with N/O stack.