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Comparison of the Interconnect Capacitances of Various SRAM Cell Layouts To Achieve High Speed, Low Power SRAM Cells

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1. Introduction

Many studies that deal with the smallest SRAM cell size have been reported [1,2]. This is because the reduction of the SRAM cell size is inevitable for the achievement of System on Chip devices with fine operation. However, these challenges have been independently applied to different SRAM cell layouts [3]. In this study, based on our design rules for 90 nm CMOS technology, we have designed various SRAM cell layouts and derived interconnect capacitances for each memory cell. A 3 dimensional (3D) interconnect simulator (Raphael) [4,5], which gives more accurate capacitance values than conventional 2D simulators, was employed. By showing that the simulated bit line (BL) interconnect capacitance (C_{BL}) is in good accordance with the measurement result, we quantitatively clarify that an SRAM cell with a smaller C_{BL} is suitable for realizing low power and high speed SRAMs.

2. Interconnect Capacitances for Various SRAM Cells

We can categorize SRAM cell layouts into 2 types. Fig.1 shows various layouts under the first metal layer (1M). One of them is the Parallel Gate Structure (PGS) where the gates are aligned in the same direction (Fig.1a), and the other is the Orthogonal Gate Structure (OGS) where the gate layers are orthogonal to each other (Figs.1b and 1c). We can realize two types of BL configuration for PGS: one has the BL in the second metal layer (PGS_2M), and the other in the third metal layer (PGS_3M). As for the OGS, we can furthermore categorize the cell into 2 types: OGS_2M and OGS_3M, as shown in Fig.1. Table I summarizes these cell features. Each layout is drawn in our original design rule for 90 nm CMOS technology [5]. Note that PGS_2M has the smallest cell area. Fig.2 shows bird's-eye views of PGS_2M and OGS_2M. Assuming that each SRAM cell has the same dielectric layer structure, we compared the interconnect capacitances. Fig. 3 shows a cross sectional view of the fabricated chip, which we introduced to 3D simulator. Table II summarizes the simulated interconnect capacitances for each cell layout. When compared with each other, the PGS_2M has the smallest C_{BL} of all. On the other hand, OGS_2M has the smallest word line (WL) interconnect capacitance.

We applied these results to a circuit simulation (HSPICE), and estimated the BL delay and the power consumption. Here the BL delay is defined as the time for the BL swing to reach 150 mV after the pre-decode (PD) signal is activated. Fig.4 shows the normalized waveforms in the SRAM read cycle for PGS_2M and OGS_2M. It is found that, although the WL in PGS_2M is activated more slowly than that in OGS_2M, PGS_2M reduces the BL delay by 14%, compared to OGS_2M. Fig.5 shows the BL voltage dependence on the power consumption. Compared to OGS_2M, PGS_2M reduces the power by 30%, providing that the sense amplifier detects the BL voltage difference at 150 mV. Therefore, we can conclude that the C_{BL} plays the most important role in achieving high speed and low power SRAMs.

3. Experimental Results for 256 Kbit PGS_2M SRAM

Fig.6 is a chip microphotograph of a 256 Kbit SRAM of the PGS_2M type. Fig. 7 shows Shmoo plot of our test chip. The measured access time is 3.0 ns at a Vdd of 1.2 V and at room temperature.

In our test chip, we designed the sense enable signal so that it was arbitrarily generated. This enables us to measure C_{BL} as explained below. Fig.8 shows the sense enable timing dependence of the power consumption in the 256 Kbit cell array. The power increases as the sense enable timing is delayed. The saturated power indicates that the BL voltage swings fully from 1.2 V to 0 V. In this situation, the power consumption can be expressed by $P = C_m f V_{dd}^2$, where C_m represents the capacitance, f the operation frequency, and V_{dd} the supply voltage. Note that C_m contains not only C_{BL} but also the contribution of the access transistors connected to the discharging BL, i.e. the gate overlap capacitance and the junction capacitance. By subtracting these effects from C_m, we can measure C_{BL}. As a result, the error between the simulated result and the measured one was found to be +3.7% on average (Fig.9). Therefore, it was verified that our result obtained by 3D simulator was quite reliable.

4. Comparison between PGS and OGS

By using the circuit diagram which corresponds to the layout of Fig. 6, we estimated the access time and the power consumption for PGS_2M, OGS_2M and OGS_3M 256 Kbit SRAMs. Here we assumed that the interconnect capacitance in the peripheral circuits of OGSs was modified in accordance with each cell type. Fig.10 shows a comparison of the access times for each cell. To see the effect of the peripheral circuits, we divided the access time into three parts; from clock to WL, from WL to sense amplifier enable (SAE) and from SAE to data out (DO). The WL-SAE contribution, which is mainly affected by C_{BL} dominates most of the access time, so that PGS_2M with the smallest C_{BL} is the fastest of all. Compared to OGS_3M, PGS_2M reduces the access time by 16.7%. Fig.11 shows the simulated result for the active power. The power consumption in PGS_2M becomes 19.7% less than that in OGS_3M. Consequently, PGS_2M is found to be the most suitable for realizing low power and high speed SRAMs.

5. Conclusions

In this study, through the analysis of the interconnect capacitance, we quantitatively confirmed that the SRAM with PGS_2M was superior to that with OGS, providing that all the design rules were the same. By using PGS_2M, the power consumption was reduced by 19.7% and the operation was 16.7% faster, compared to OGS_3M.

References

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[2] S. –M. Jung et al., IEDM Tech. Dig. p. 419, 2002.
[3] M. Ishida et al., IEDM Tech. Dig. p. 908, 1998.
[4] http://www.avanticorp.com
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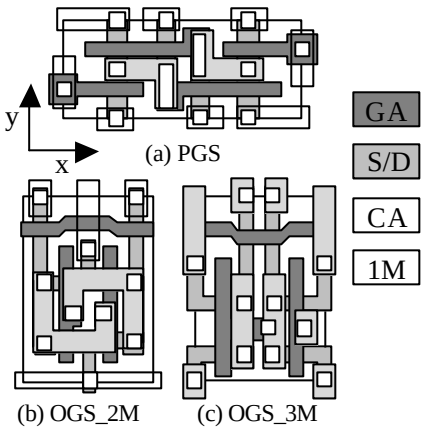


Fig. 1 Various SRAM cell layouts.

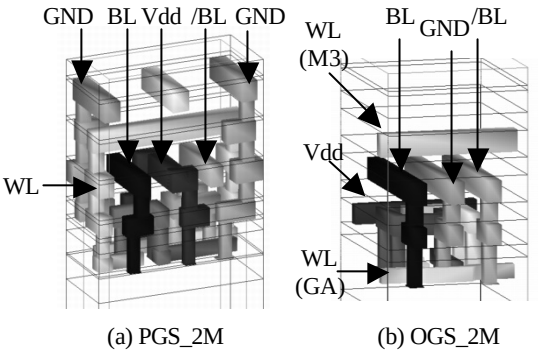


Fig. 2 3D graphics for PGS_2M and OGS_2M.

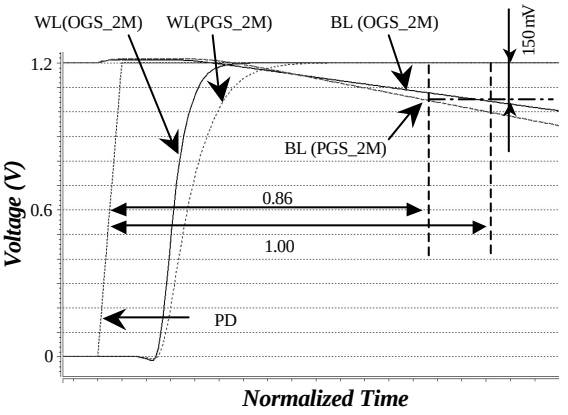


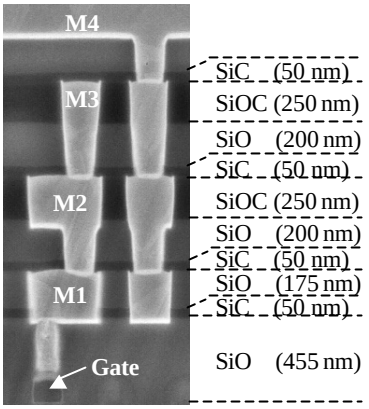
Fig. 4 Simulated waveform in read cycle.

Table I. SRAM Cell Features.

Cell Type	**PGS_2M**	**PGS_3M**	**OGS_2M**	**OGS_3M**
Bit Line	2 metal	3 metal	2 metal	3 metal
Word Line	3 metal	2 metal	poly, 3 metal	poly, 2metal
X-Size (μm)	1.74	1.74	1.02	0.94
Y-Size (μm)	0.72	0.72	1.34	1.34
Area (μm^2)	1.2528	1.2528	1.3668	1.2596

Table II. Estimated interconnect capacitance for each cell (fF/unit memory cell).

	Bit Line	Word Line
PGS_2M	0.230	0.696
PGS_3M	0.288	0.684
OGS_2M	0.359	0.300
OGS_3M	0.413	0.334



Material	*Dielectric Constant*
SiO	4.3
SiC	4.8
SiOC	2.8

Fig. 3 Micrograph of the cross sectional view for dielectric layer and metal structure.

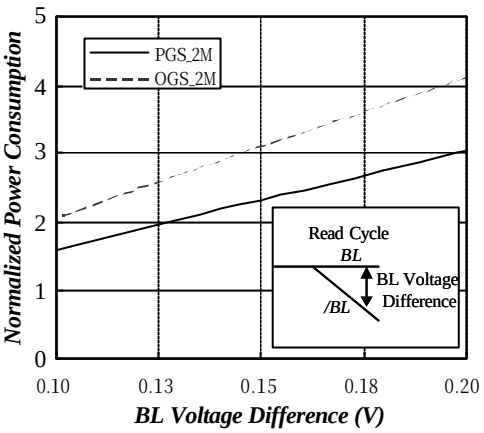


Fig. 5 Dependence of the power consumption on BL voltage difference.

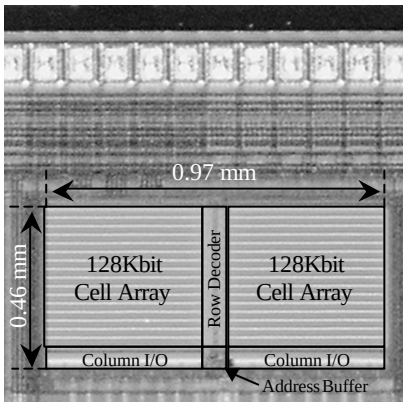


Fig. 6 Microphotograph of 256 Kbit SRAM.

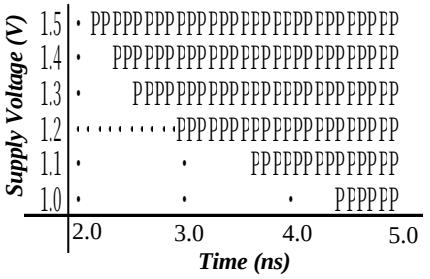


Fig. 7 Shmoo plot for 256 Kbit SRAM.

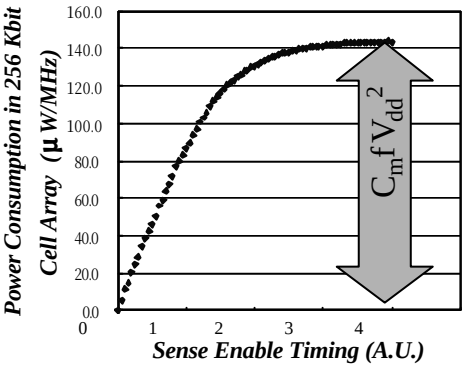


Fig. 8 Dependence of active power on SE timing (measured).

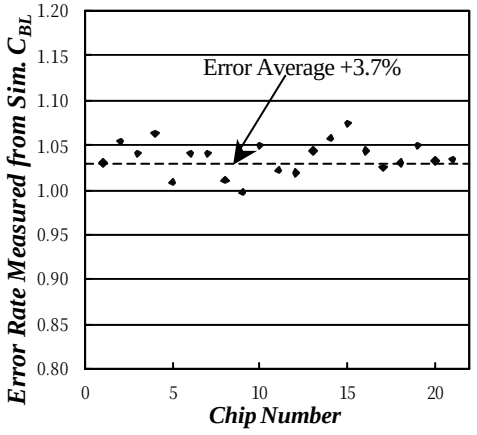


Fig. 9 Fluctuation of measured C_{BL}. 1.00 in the vertical axis means the simulated value shown in Table II.

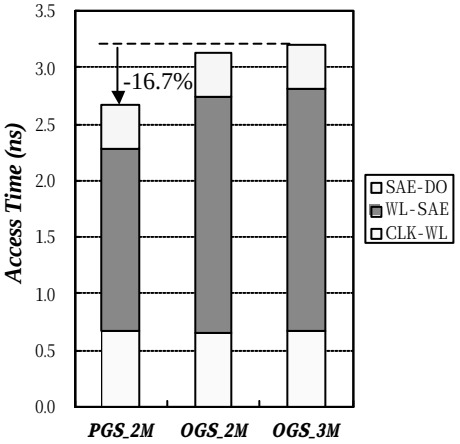


Fig. 10 Comparison of access times.

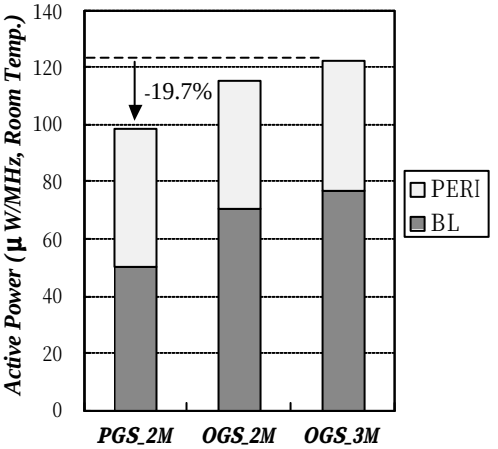


Fig. 11 Comparison of power consumptions.