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Eliminating Threshold Voltage Offset of PMOSFETs in High-Density DRAM

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1. Introduction

This paper presents, for the first time, both the principles and experimental results concerning the elimination of the threshold voltage (V_{th}) offset of a pair P+gate PMOSFET in a high-density DRAM. The poor performance of the cross-couples in DRAM sense amplifiers is caused by the V_{th} offset which is defined as the statistical average of the V_{th} difference between a pair MOSFET (Figs. 1 and 2). In the present study, the V_{th} offset increases with the increasing DRAM density, particularly, in the case of PMOSFETs (Fig. 3). Moreover, the principles of the V_{th} offset characteristic of PMOSFETs are shown, and the V_{th} offset is successfully reduced.

2. Principles

It has been reported that the V_{th} shifts of NMOSFETs are caused by the parasitic effects such as depletion of channel dopant and stress induced at the shallow trench isolation (STI) edge [1]. However, the V_{th} offset of PMOSFETs in a G bit-scale DRAM (20 mV) is much more than the V_{th} offset of NMOSFETs (<5 mV). This paper presents a new theory for the V_{th} offset of PMOSFETs. Namely, it considers that the V_{th} offset of P+gate PMOSFETs is associated with phosphorus channel dopant. In particular, phosphorus tends to segregate by forming gate oxides, which enhances the V_{th} of the PMOSFETs.

It is assumed that the strong V_{th} enhancement occurred at the STI edges. The STI edges are rounded and can be considered as a group of (hkl) crystal planes. According to the Deal-Groove model of oxidation, a gate oxide at an STI edge becomes thicker than that at a flat plane (001); the thicker gate oxides enhance the threshold voltage. A comparison between the V_{th} shifts of an NMOSFET and a PMOSFET is shown in Table. 1. The combination of channel-dopant segregation and thicker gate oxides at the STI edge increases the V_{th} enhancement of PMOSFETs.

The degree of the V_{th} enhancement is determined by the shape of STI edge. Because the STI formation by dry etching cannot be uniform, the shape of STI edge changes with the size of STI. This results in the difference in the STI shape between two pair MOSFETs（Fig. 4）. The V_{th} offset is generated when the gate electrodes are located on the different STI edges. The V_{th} offset of PMOSFETs increases because the layout of the U-shaped gate electrodes is not allowed to be symmetric with respect to STI in a high-density DRAM.

3. Device Fabrication

MOSFETs were made by STI followed by channel-ion implantation. A poly-metal gate electrode was fabricated on 3.5-nm-thick NO gate oxides. The length and width of the U-shaped gate electrodes were 0.24 μm and 1.54 μm, respectively. The threshold voltage was measured at a drain current of 10nA with a drain voltage of | 1.4 | V. The V_{th} of 207 pair MOSFETs were measured, and the V_{th} offset was obtained.

4. Results and Discussion

The effect of channel dopant on the V_{th} offset is shown in Fig. 5. This figure compares the V_{th} offset of PMOSFETs with and without phosphorus channel-ion implantation. With the ion implantation, the V_{th} offset is about 20 mV; without the ion implantation, the V_{th} offset is negligibly small because the phosphorus segregation is insignificant. This result suggests that the V_{th} offset of PMOSFETs is caused by the channel-dopant segregation as shown in Table 1.

The effect of STI width on the V_{th} offset is shown in Figs. 6 and 7. The V_{th} offset of the NMOSFETs is less than 5 mV and independent of the STI width (Fig. 6). However, the V_{th} offset of the PMOSFETs is generated (20 mV) with increasing STI width ($L_{up} > L_{down}$) (Fig. 7). These results indicate that the V_{th} offset of PMOSFETs is strongly influenced by the STI edge. Accordingly, the V_{th} offset can be eliminated by setting L_{up} equal to L_{down}.

5. Conclusions

The principles of the V_{th} offset of PMOSFETs were given, and the V_{th} offset was experimentally eliminated from 20 mV to zero by controlling the phosphorus concentration and the layout of cross-couples in sense amplifiers. It is expected that the reduction of the V_{th} offset will improve the retention time of a G bit-scale DRAM [2].

References

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[2] R. Takemura, T. Sekiguchi, H. Fujisawa, T. Takahashi, T. Sakata, and M. Nakamura, SSDM2001, pp. 102-103.

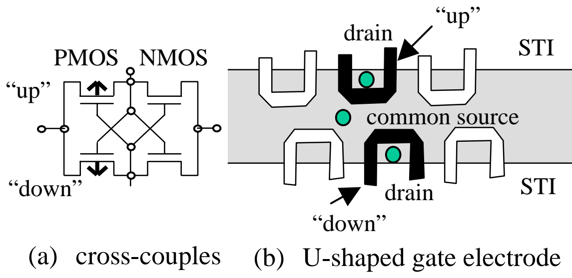

Fig. 1: Pair-MOSFETs in cross couples of sense amplifiers

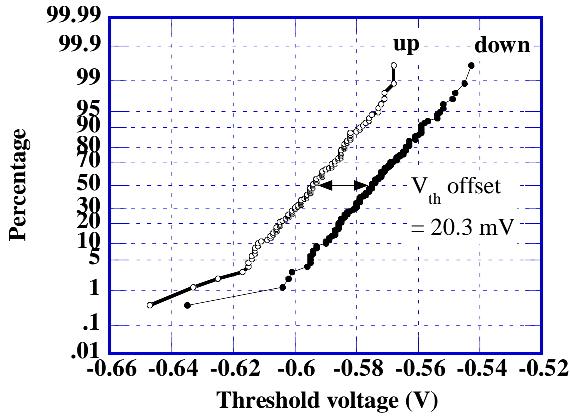

Fig. 2: Cumulative distributions of threshold voltage of pair PMOSFETs

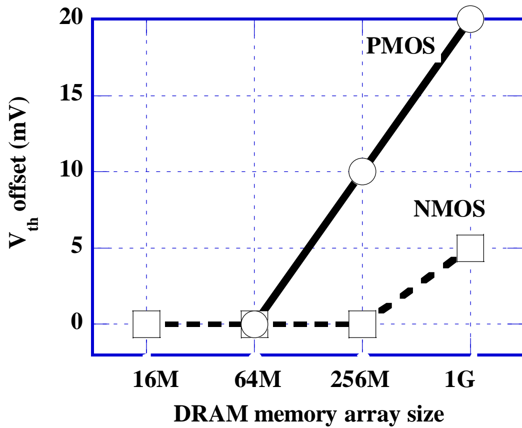

Fig. 3: Trend in V_{th} offset of pair MOSFETs

Tab. 1: Parasitic V_{th} shift at STI edge

type	parasitic effects at STI edge		total
	gate oxide	channel dopant	
PMOS	⬆ (thicker)	⬆ (P segregation)	⬆ ⬆
NMOS	⬆ (thicker)	⇩ (B depletion)	⬆ ⇩

⬆ indicates V_{th} enhancement ⇩ indicates V_{th} depletion

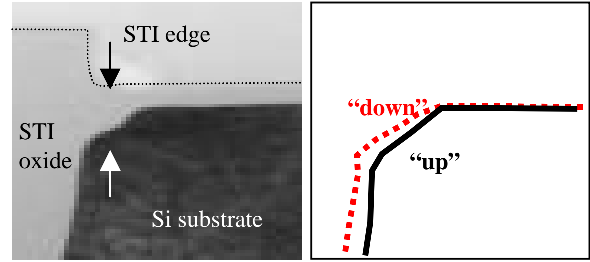

Fig. 4: Shape of STI edge

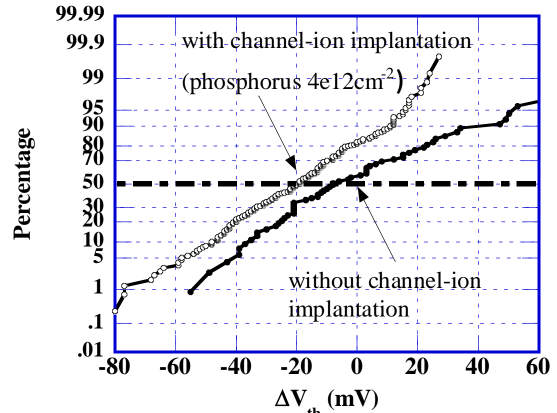

Fig. 5: Effect of P-channel dopant concentration on V_{th} offset of PMOSFETs. $\Delta V_{th} = V_{th}^{up} - V_{th}^{down}$

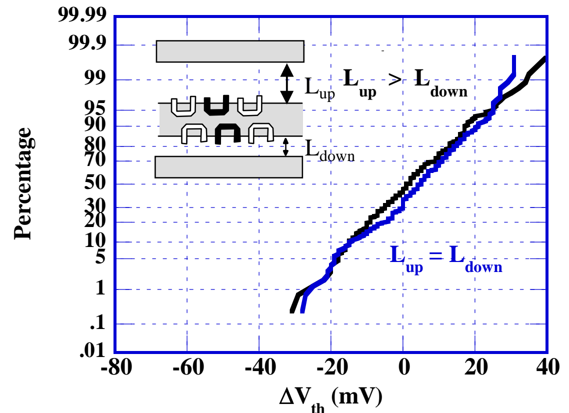

Fig. 6: Effect of STI width on V_{th} offset of NMOSFETs

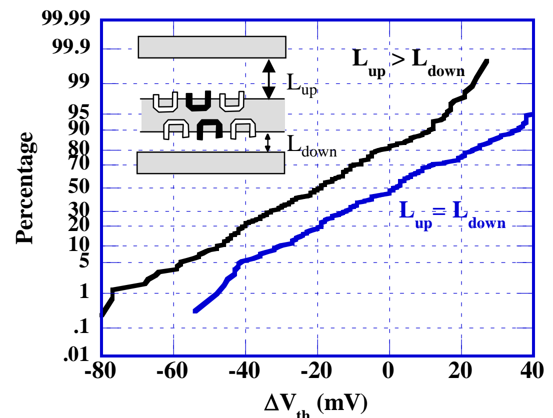

Fig. 7: Effect of STI width on V_{th} offset of PMOSFETs