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Gate Engineering to prevent NMOS Dopant Channeling for Nano-Scale CMOSFET Technology

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1. Introduction

As device sizes are scaled down to deep submicron region, SALICIDE (Self-Aligned silicide) of gate and source/drain is indispensable to increase drive capability by reducing sheet resistance of the source/drain region and contact resistance. Unfortunately, Salicide process may induce undesirably large junction leakage current because of the shallow junctions after silicidation. To reduce leakage current, an arsenic and phosphorus double ion implanted (co-implant) source/drain junction is proposed [1]. Also, as the gate oxide thickness gets shrunk aggressively, it is highly necessary to increase gate doping as high enough as possible for the lower poly depletion effect and high performance device characteristics without degradation of gate oxide. It is known that the gate poly-Si with larger grain size is desirable in order to increase the gate doping efficiency [2]. Meanwhile, phosphorus (P) atoms that are generally implanted on the gate poly-Si prior to the gate formation enhance the grain growth of the gate poly-Si during the crystallization [3]. However, occasionally, we happened to see an abnormal transistor characteristic in nano-scale MOSFETs, such as nMOS off-state current (Ioff) fluctuation. The points of Ioff fluctuation also showed the hump property. The aim of this paper is to characterize the origin of Ioff fluctuation and to propose how to avoid the off-state current fluctuation without degradation of MOSFET performance.

2. Experimental

The NMOS transistor in this study was fabricated as follows. After formation of shallow trench isolation and twin well, the dual gate oxides of 5 and 2 nm were grown. Then, 200 nm columnar poly-Si was deposited and the gate electrode was defined using KrF stepper. After formation of source/drain extension regions and Si_3N_4 sidewall, the source and drain were formed by double ion implantation (As : 50keV/5×10^{15} cm^{-2}, Ph : 35keV/3×10^{13} cm^{-2}). Sequence of As and Ph implantation is split as As + Ph or Ph + As. Finally, RTP annealing (1050℃ for 10sec) was followed by $CoSi_2$ formation. Detail of the process flow is shown in Fig.1.

3. Results and discussion

Fig. 2 shows the dependence of junction leakage current on the sequence of As and Ph implantation. Ph first implantation is much effective in reducing the junction leakage current mainly due to the deeper Ph profile as in Fig. 3. However, Ph first implantation sometimes showed abnormal off-state current fluctuation, while no fluctuation in case of As first implantation as shown in Fig. 4. The point of large off-state current showed the hump at the sub-threshold region as in Fig. 5. Moreover, it is shown that GOI characteristics of Ph + As case degrades as in Fig. 6. Therefore, Ph + As scheme is undesirable for MOSFET viewpoint in spite of improved junction leakage characteristics.

To explain this anomalous behavior, channeling through poly crystalline silicon gate was proposed. It is said that the poly silicon grain structure plays a major role in its interface roughness with the gate oxide [4]. Fig. 7 shows the structure of the columnar poly silicon with and without Ph doping of gate poly before patterning of gate. The grain size is influenced a lot by Ph doping as in Fig. 7. It can be thought that Ph channeling may happen during the Ph implantation in case of Ph + As due to the large grain size. In case of As + Ph, there is no Ph channeling because the poly layer becomes amorphous by As implantation. Fig. 8 shows schematically the mechanism of Ph dopant channeling through polycrystalline silicon grain boundary in source/drain implantation process. The phosphorus atoms channel through the gate poly silicon as shown in Fig. 8(a) while As implantation makes the poly silicon surface amorphous silicon as in Fig. 8(b). In case of without Ph doping before gate definition, there no Ioff fluctuation in spite of Ph + As scheme as shown in Fig. 9. Fig. 10 shows the Ioff fluctuation phenomena although Ph implantation energy and anneal temperature is wide varied. Hence, formation of amorphous layer on the top area of gate poly is highly necessary. We proposed 2-layer poly structure, that is, amorphous top layer and columnar bottom layer. As shown in Fig. 11, stacked poly structure is very efficient in suppressing Ioff fluctuation.

4. Conclusions

In conclusion, we investigate the anomalous behavior of off-state current fluctuation by the phosphorous atom channeling through the gate poly silicon during source/drain implantation. It is shown that large grain size is a main cause of channeling. It is also shown that stacked poly structure is highly efficient in suppressing Ph channeling without degradation of device performance such as Ion-Ioff characteristics and junction leakage current.

References

[1] H-D Lee et al, IEEE Electron Device Letters, 42 (1999).
[2] H.P. Tuinhout et al., IEDM Tech. Digest, 631 (1997).

[3] H. Ito, et al, IEDM Tech. Dig., 635 (1997). (2001).
[4] Avid Kamgar, et al., IEEE Electron Device Letters,22

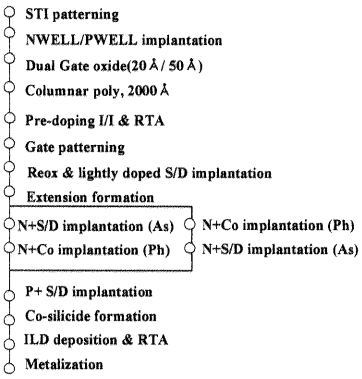

Fig. 1. Process flow for experiment.

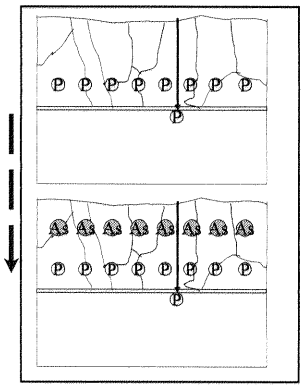

Fig. 8(a). Schematic diagram of Ph channeling in Ph + As scheme.

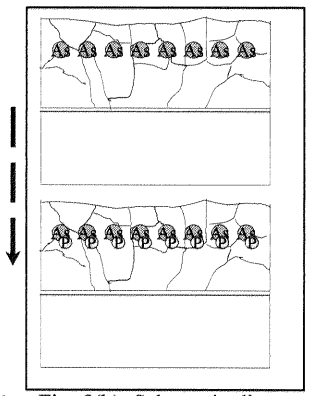

Fig. 8(b). Schematic diagram of Ph channeling in As + Ph scheme.

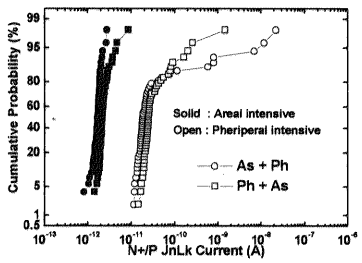

Fig. 2. Dependence of n+/p junction leakage current on the As and Ph implantation scheme.

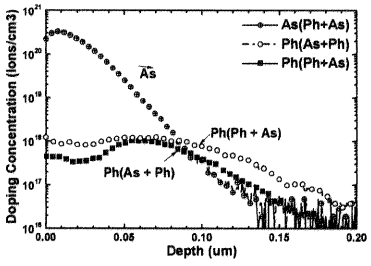

Fig. 3. SIMS profile of As and Ph for As + Ph and Ph + As schemes.

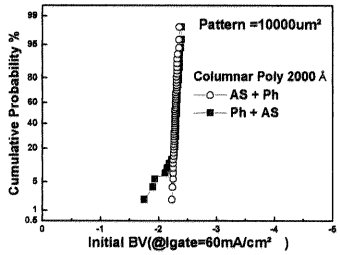

Fig. 6. Dependence of GOI characteristics on the As and Ph implantation scheme.

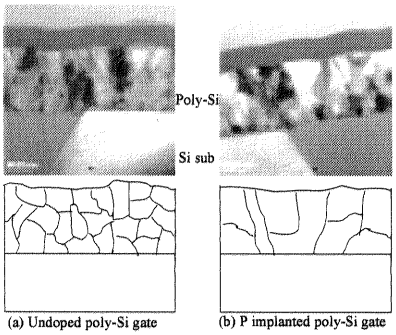

Fig. 7. TEM photographs of poly-Si gate.

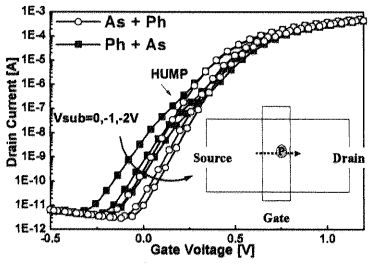

Fig. 5. Ids vs. Vgs characteristics. Ioff fluctuation point of Ph + As case shows hump property in subthreshold region.

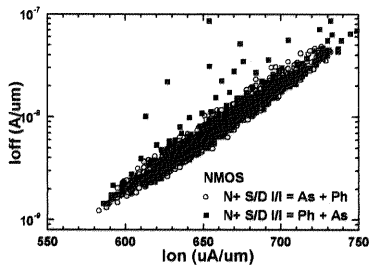

Fig. 4. Ion vs. Ioff characteristics. Ph + As scheme shows Ioff fluctuation.

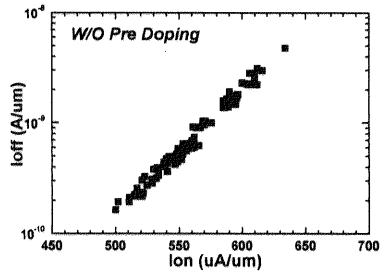

Fig. 9. Ion vs. Ioff characteristics in case of without Ph doping prior to gate definition.

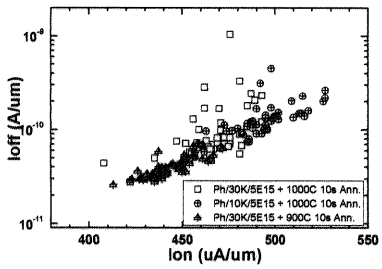

Fig. 10. . Ion vs. Ioff characteristics for various Ph doping condition.

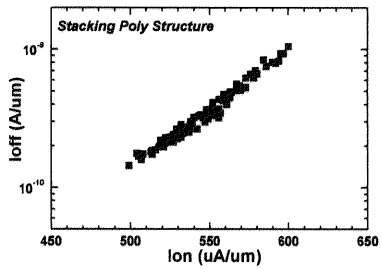

Fig. 11. Ion vs. Ioff characteristics of stacked poly structure.